
EM78M611E

**8-Bit
Microcontroller**

**Product
Specification**

DOC. VERSION 0.9

ELAN MICROELECTRONICS CORP.

March 2006



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Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2006/03/03

PRELIMINARY



1 General Description

The EM78M611E is an integrated USB MTP controller IC. It has a built-in USB transceiver, built-in 4-bit EEPROM, built-in PWM function and built-in AD converter. The EM78M611E can be a USB & PS/2 Keyboard & Mouse controller.

2 Feature

- n Fully compliant with the Universal Serial Bus Specification, version 1.1
- n USB keyboard design is compliant with USB Device Class Definition for Human Interface Device (HID), Firmware Specification, and version 1.1
- n Two 8-bit transmit FIFOs
- n One 8-bit bidirectional FIFO
- n 6K × 13 on-chip Program ROM
- n 144 bytes of General Purpose RAM
- n 11 LED direct sink pins with internal serial resistor (P70-P72, P76-P77, P90-P93, P95-P96)
- n Built-in 4-bit EEPROM with a minimum of 10K write/erase cycles (achieved by F/W)
- n Built-in PWM (Pulse Width Modulation) function
- n Built-in 24 channels Analog-to-Digital converter with 10-bit resolution
- n 8-level stack for subroutine nesting
- n RC Oscillator with internal RC
- n Ports 5, 6, 8, 9, P74~P77 with pull-up resistors
- n Wake-up pins in Ports 6, 9, P74~P77
- n Operates at 6MHz or 12MHz frequency
 - 6MHz Frequency: 2.5V~5.5V
 - 12MHz Frequency: 4.0V~5.5V only
- n Available in 40-pin DIP, 44-pin QFP, 20-pin PDIP/SOP/SSOP, 24-pin PDIP/SOP
- n Built-in 20MHz Low Pass Filter in Oscillator (maximum MCU frequency is 12MHz)

3 Applications

- n USB Keyboard only
- n Keyboard switch with USB or PS/2
- n USB keyboard with PS/2 mouse port
- n USB joystick

4 Pin Configuration (Package)

P70~P77 are high voltage I/O pins. All the rest are low voltage I/O pins.

For EM78M611EXAP (40-pin DIP), P95, P96, P76, P77 are set as output pins.

VSS	1	I	40	OSCO
V3.3	2		39	OSCI
VP / CLK / P74	3		38	VDD
VM / DATA / P75	4		37	P70
P90	5		36	P71
P91	6		35	P72
P92 / PWM1 / SE1	7		34	P67 / AD23
P93 / PWM2 / SE2	8		33	P66 / AD22
P94/Vpp	9		32	P65 / AD21
VNN	10		31	P64 / AD20
P50 / AD0	11		30	P63 / AD19
P51 / AD1	12		29	P62 / AD18
P52 / AD2	13		28	P61 / AD17
P53 / AD3	14		27	P60 / AD16
P54 / AD4	15		26	P87 / AD15
P55 / AD5	16		25	P86 / AD14
P56 / AD6	17		24	P85 / AD13
P57 / AD7	18		23	P84 / AD12
P80 / AD8	19		22	P83 / AD11
P81 / AD9	20		21	P82 / AD10

Figure 1 40-pin DIP Pin Configuration of EM78M611EXAP

EM78M611EXAQ (44-pin QFP)

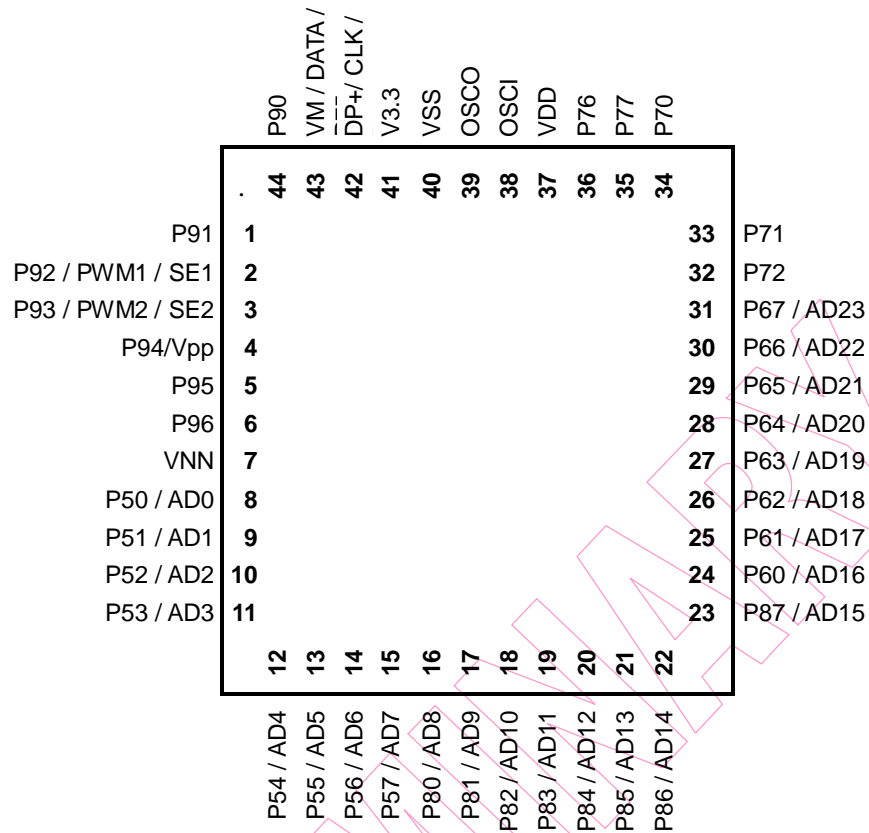


Figure 2 44-pin QFP Pin Configuration of EM78M611EXAQ

EM78M611EXBP/BM/DM (20-pin PDIP/SOP/SSOP)

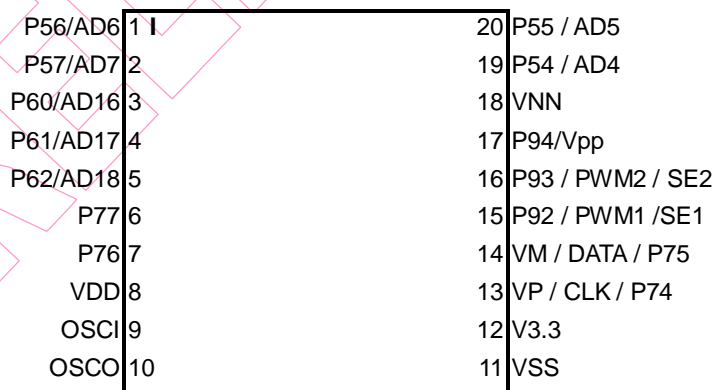


Figure 3 20-pin PDIP/SOP/SSOP Pin Configuration of EM78M611EXBP/BM/DM

EM78M611EXCP/CM/EM (24-pin PDIP/SOP/SSOP)

OSCO	1	24	OSCI
VSS	2	23	VDD
V3.3	3	22	P76
VP / CLK / P74	4	21	P77
VM / DATA / P75	5	20	P66 / AD22
P92 / PWM1 / SE1	6	19	P65 / AD21
P93 / PWM2 / SE2	7	18	P64 / AD20
P94/Vpp	8	17	P63 / AD19
VNN	9	16	P62 / AD18
P54 / AD4	10	15	P61 / AD17
P55 / AD5	11	14	P60 / AD16
P56 / AD6	12	13	P57 / AD7

Figure 4 24-pin PDIP/SOP/SSOP Pin Configuration of EM78M611EXCP/CM/EM

PRELIMINARY

5 Functional Block Diagram

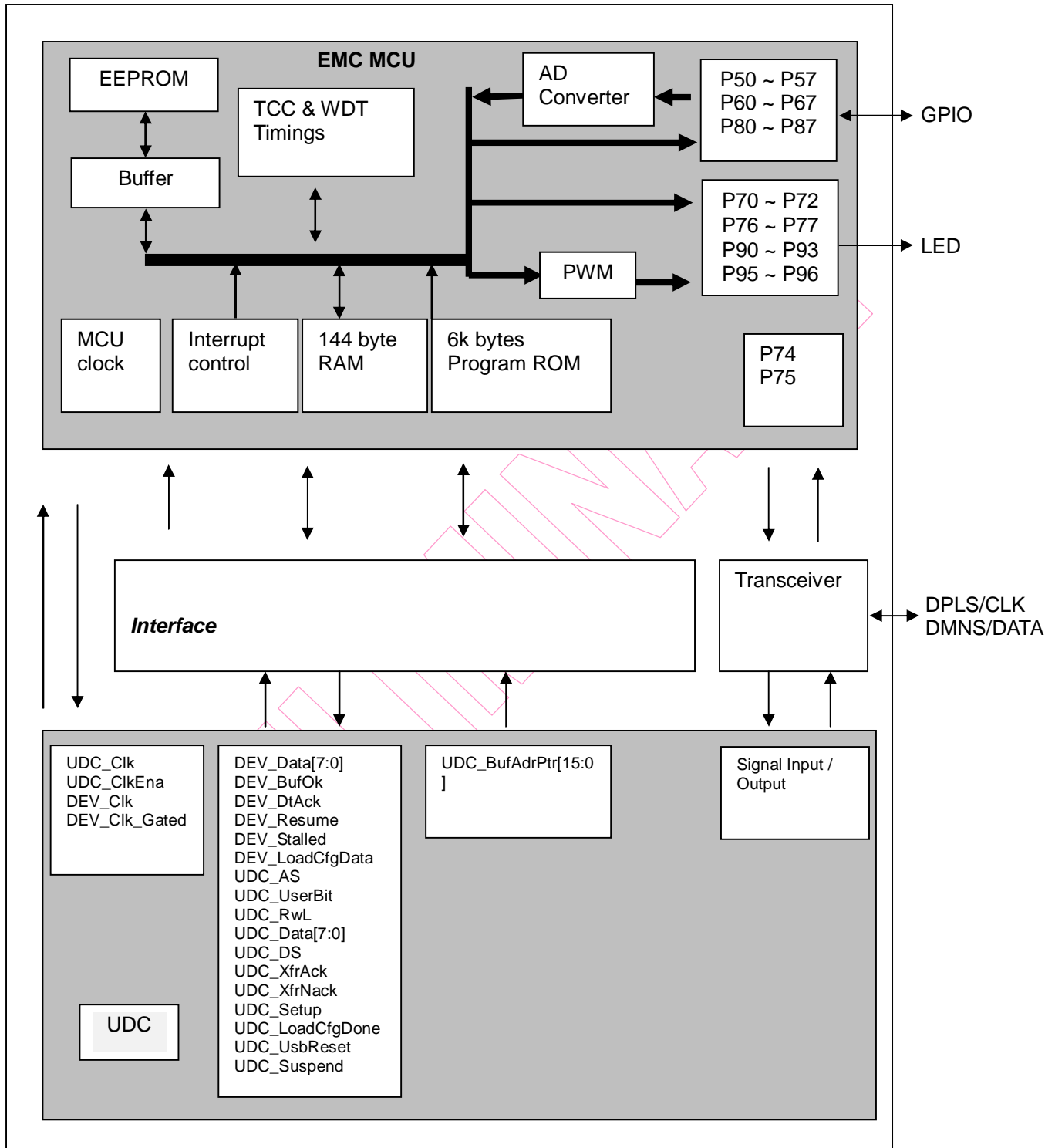


Figure 5 Functional Block Diagram

6 Pin Description

Symbol	I/O	Function
P50 ~ P57	I/O	Port 5 is an 8-bit Low Voltage (3.3V) bidirectional I/O port. They can be pulled-high internally by software control.
AD0~AD23	I	Analog to Digital Converter
P60 ~ P67	I/O	Port 6 is an 8-bit Low Voltage (3.3V) bidirectional I/O port. They can be pulled-high internally by software control.
P80 ~ P87	I/O	Port 8 is an 8-bit Low Voltage (3.3V) bi-directional I/O port. They can be pulled-high internally by software control.
P90~P93, P95~P96	I/O	Port 9 is a 6-bit Low Voltage (3.3V) bidirectional I/O port. They can be pulled-high internally by software control. P90-P93, P95-P96 are LED direct sink pins.
PWM1~PWM2 (P92~P93)	O	PWM output pins
RF1~RF2 (P92~P93)	I	RF signal catching pins
P70~P72,P76,P77	I/O	LED direct sink pins. P76, P77 can be pulled-high internally. High Voltage (5V)
VP/ CLK(P74)	I/O	USB plus data line interface or CLK of PS/2 keyboard. It can be pulled-high internally by setting in PS2 mode. High Voltage (5V) .
VM/ DATA(P75)	I/O	USB minus data line interface or DATA of PS/2 keyboard. It can be pulled-high internally by setting in PS2 mode. High Voltage (5V) .
OSCI	I	Crystal input
OSCO	O	Crystal output
VDD	PWR	Power supply pin
GND	PWR	Ground pin
VNN	I	MTP program pin
P94/Vpp	I	Input only I/O. Vpp in MTP programming.
V3.3	PWR	3.3V output

7 Function Description

7.1 Operational Registers

7.1.1 R0 (Indirect Addressing Register): default (0b0000_0000)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

7.1.2 R1 (TCC): default (0b0000_0000)

Incremented by the instruction cycle clock.

Written and read by the program as any other register.

7.1.3 R2 (Program Counter) & Stack

Depending on the device type, R2 and hardware stack are **13 bits wide**.

The structure is depicted in Fig. 3.

Generates **6K** × 13 on-chip ROM addresses of the relative programming instruction codes. One program page is 1K words long.

R2 is set all "0"s upon a RESET condition.

"JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows jump to any location on one page.

"CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be any location on one page.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.

"ADD R2,A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC are cleared.

Any instruction which writes to R2 (e.g. "ADD R2, A", "MOV R2,A", "BC R2,6",.....) (except "TBL") will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.

"TBL" allows a relative address to be added to the current PC (R2+A→R2), and the contents of the ninth and tenth bits (A8~A9) of the PC are not changed. Thus, the computed jump can be on the second (or third, or fourth) 256 locations in one program page.

The most significant bits (A10~A12) will be loaded with the contents of bit PS0~PS2 in the status register (R3) upon the execution of a "JMP", "CALL", or any instruction which writes to R2.

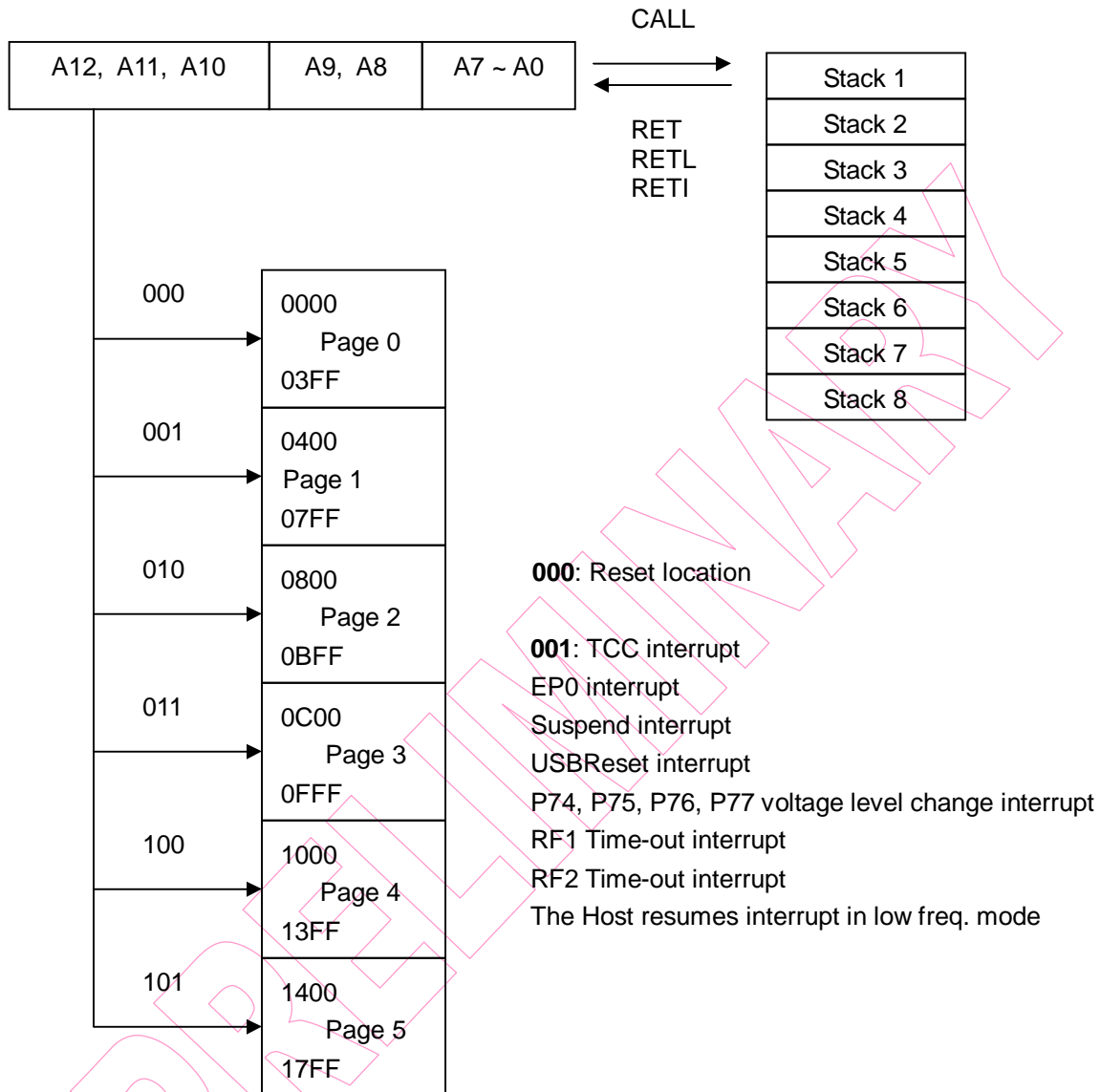


Figure 7-1 Program Counter Organization

7.1.4 R3 (Status Register): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS2	PS1	PS0	T	P	Z	DC	C

Bit 0 (C) Carry flag

Bit 1 (DC) Auxiliary carry flag

Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Bits 5 (PS0) ~ 7 (PS2) Page select bits. PS0~PS2 are used to pre-select a program memory page. When executing a "JMP", "CALL", or other instruction which causes the program counter to be changed (e.g. MOV R2,A), PS0~PS2 are loaded into the 11th, 12th and 13th bits of the program counter, selecting one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS2 bits. That is, the return will be always to the page from where the subroutine was called, regardless of the current setting of PS0~PS2 bits.

PS2	PS1	PS0	Program Memory Page [Address]
0	0	0	Page 0 [0000-03FF]
0	0	1	Page 1 [0400-07FF]
0	1	0	Page 2 [0800-0BFF]
0	1	1	Page 3 [0C00-0FFF]
1	0	0	Page 4 [1000-13FF]
1	0	1	Page 5 [1400-17FF]

7.1.5 R4 (RAM Select Register): default (0b0000_0000)

Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.

Bits 6~7 determine which bank is activated among the 4 banks.

If no indirect addressing is used, the RSR can be used as an 8-bit wide general purpose read/write register.

See the configuration of the data memory in Fig 7-2.

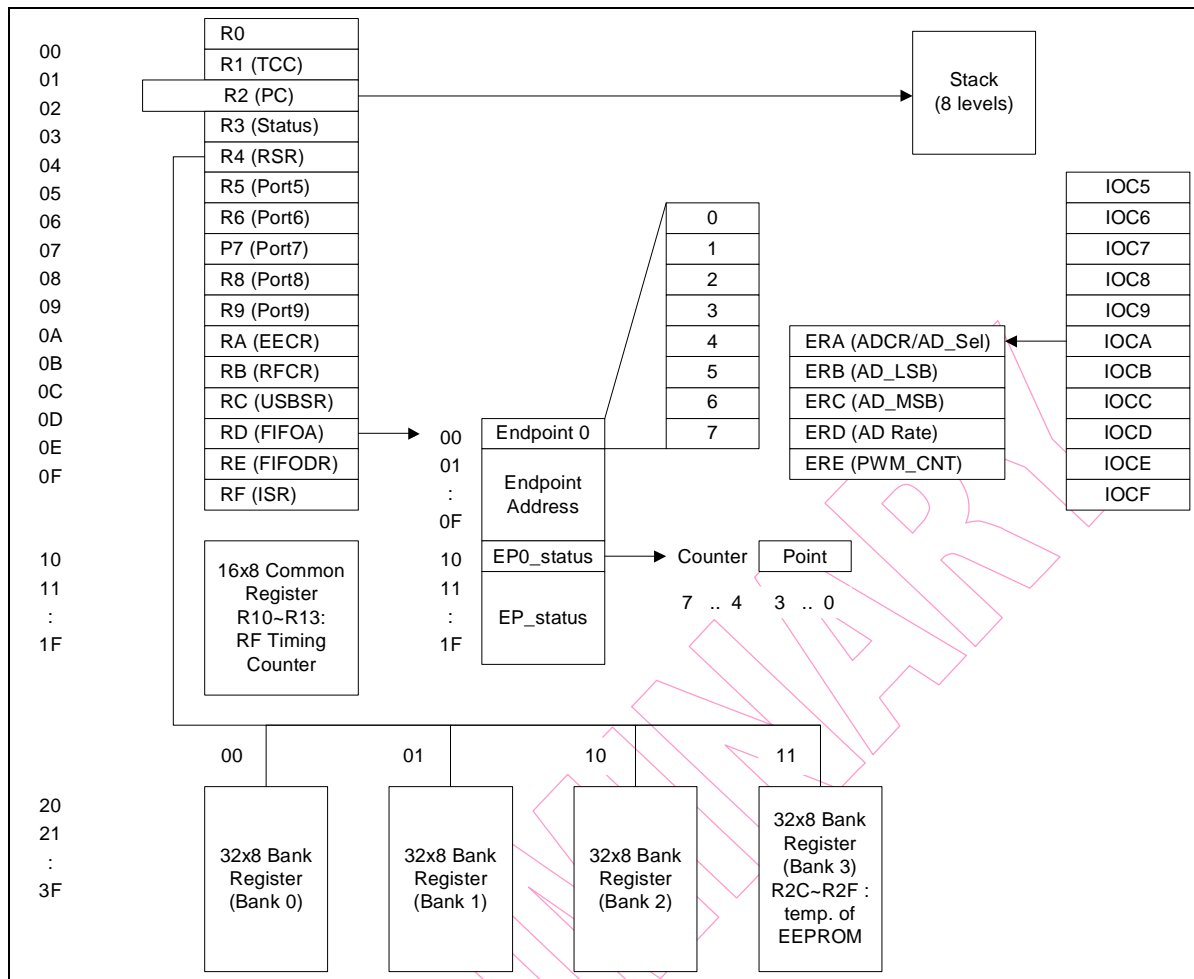


Figure 7-2 Data Memory Configuration

7.1.6 R5~R9 (Port 5 ~ Port 9): default (0b0000_0000)

Five 8-bit I/O registers.

P75 read/write data from the Data pin. P74 read/write data from CLK pin.

P70 ~ P72, P76, P77, P90 ~ P93, P95 ~ P96 control LED.

7.1.7 RA (EEPROM Control Register): default (0b0000_0011)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_A4	EE_A3	EE_A2	EE_A1	EE_A0	EE_O.K.	EE_C1	EE_C0

Bit 1, 0 (EE_C1, EE_C2): EEPROM control bits. Set by software. Hardware activates immediately when these bits are set. This register would be general register if the EEPROM function is disabled in MTP code option.

00: Read data from EEPROM to R2C~R2F of Bank 3

01: Write data from R2C~R2F of Bank 3 to EEPROM (After Writing data to EEPROM, hardware has to read data from EEPROM to R2C~R2F of Bank 3)

10: Erase EEPROM

11: Disable any active to EEPROM

Bit 2 (EE_O.K.): EEPROM activate O.K. bits. Hardware has to set this bit, when the data of R2C~R2F of Bank 3 and the temp Register of writing data are the same

0: not the same

1: the same

Bits 7~3 (EE_A4~EE_A0): EEPROM address

7.1.8 RB (RF Control Register): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2~ Bit 0
RF_PAT1	RF_PAT0	RF2	RF1	RF0	RF_DBN

Bit 2~Bit 0 (RF_DBN): These are used for defining de-bounce times in RF pattern detecting application.

Bit 3 (RF0) ~ Bit 5 (RF2): RF Timing prescaler bits

RF2	RF1	RF0	Timing Rate	6MHz (Time Count)	12MHz (Time Count)	256kHz (Time Count)
0	0	0	1:1			400μs (102.4), 800us (204.8)
0	0	1	1:2			1600μs (204.8)
0	1	0	1:4	100μs (150), 150μs (225)		
0	1	1	1:8	200μs (150)	100μs (150), 150μs (225)	
1	0	0	1:16	400μs (150)	200μs (150)	
1	0	1	1:32	800μs (150), 1000μs (187.5), 1200μs (225)	400μs (150)	
1	1	0	1:64	1600μs (150), 2000μs (187.5), 2400μs (225)	800μs (150), 1000μs (187.5), 1200μs (225)	
1	1	1	1:128	3200μs (150), 4000μs (187.5), 4800μs (225)	1600μs (150), 2000μs (187.5), 2400μs (225)	



Bit 6 (RF_PAT0): The pattern counter interrupt flag of the 1st RF module.

- 0: Low Pattern compare interrupt
- 1: High Pattern compare interrupt

Bit7 (RF_PAT1): The pattern counter interrupt flag of the 2nd RF module.

- 0: Low Pattern compare interrupt
- 1: High Pattern compare interrupt

7.1.9 RC (USB Application Status Register): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP0_W	EP0_R	EP1_R	EP2_R	EP2_W	UDC_Suspend	UDC_Writing	STALL

Bit 0 (STALL): Set by software, reset by the interface while it receives UDC_XfrNack or UDC_XfrAck from UDC. Readable and writable.

Bit 1 (UDC_Writing): read only

- 1: EP0's FIFO is currently busy. (UDC_RwL is low & UDC_AS rising in EP0)
- 0: EP0's FIFO is free for data transition. ACK, NAK reset.

Bit 2 (UDC_Suspend): UDC_SUSPEND status bit. Depends on UDC_Suspend. Read only.

Bit 3 (EP2_W): Set by interface when buffer is Ok. (the interface detects UDC_XfrAck while UDC_RwL is low), reset by software when buffer be read. If this bit is'nt reset, the interface can't assert DEV_BufOk after it detects UDC_AS. Readable and writable.

Bit 4 (EP2_R): Set by software when buffer is Ok, reset by interface when buffer is read (UDC asserts UDC_XfrAck). Readable and writable.

Bit 5 (EP1_R): Set by software when buffer is Ok, reset by interface when buffer is read (UDC asserts UDC_XfrAck). Readable and writable.

Bit 6 (EP0_R): Set by software when buffer is Ok, reset by interface when buffer is read (UDC asserts UDC_XfrAck). Readable and writable.

Bit 7 (EP0_W): Set by interface when buffer is Ok. (the interface detects UDC_XfrAck while UDC_RwL is low), reset by software when buffer is read. If this bit is not reset, the interface cannot assert DEV_BufOk after it detects UDC_AS. Readable and writable.

7.1.10 RD (FIFO Address Register): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	UAD4	UAD3	UAD2	UAD1	UAD0

Bit 0 ~ Bit 4 select FIFO address

Bits 5, 6, 7 not used

7.1.11 RE (FIFO Data Register): default (0b0000_0000)

Bit 0 ~ Bit 7 are FIFO data registers

7.1.12 RF (Interrupt Status Register): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Resume_IF	RF2_IF	RF1_IF	P74/P75/P76/ P77_IF	USBReset_IF	Suspend_IF	EP0_IF	TCIF

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when TCC timer overflows, reset by software.

Bit 1 (EP0_IF): UDC interrupt flag when the data from UDC to MCU. Set when **UDC_XfrAck** and **UDC_Setup** asserted, reset by software.

Bit 2 (Suspend_IF): UDC suspend interrupt flag. Set when **UDC_SUSPEND** asserted, reset by software.

Bit 3 (USBReset_IF): USBReset interrupt flag. It will be set when the Host issues the USB Reset signal.

Bit 4 (P74/P75/P76/P77_IF): P74, P75, P76, P77 voltage level change interrupt flag. It will be set when P74 or P75 or P76 or P77 voltage level changes in PS/2 mode. It will be set when P76 or P77 voltage level changes in USB mode.

Bit 5 (RF1_IF): RF1 Timing comparison flag. The condition is described in RF Timing counter function below.

Bits 6 (RF2_IF): RF2 Timing comparison flag. The condition is described in RF Timing counter function below.

Bits 7 (Resume_IF): Host resumes interrupt flag in Low Frequency mode.

If Bit 7 (Resume_IE) of IOCF is set (enabled), the program will be interrupted when the PC resumes operation of the device. When PC resumes the device, UDC will deassert **UDC_SUSPEND** to MCU. If **UDC_SUSPEND** is deasserted by **DEV_RESUME**, it will not cause interrupt.

"1" with interrupt request

"0" non-interrupt

RF can be cleared by instruction but cannot be set by instruction.

IOCF is the interrupt mask register.



RF must be set while interrupt condition occurs even if IOCF is not set. But it cannot interrupt the program.

7.1.13 R10~R1F, R20~R3F (General Purpose Register)

R10~R1F, and R20~R3F (including Banks 0~3) are general purpose registers.

R2C~R2F of Bank 3 are temporary registers of EEPROM register. The function is described in RA.

R10~R13 are RF Timing counter registers if RF function is enabled by setting RF_function of IOCA. Otherwise, they are general register.

R10: low signal counter of the 1st RF module that inputs from P92.

R11: high signal counter of the 1st RF module that inputs from P92.

R12: low signal counter of the 2nd RF module that inputs from P93.

R13: high signal counter of the 2nd RF module that inputs from P93.

R10~R11 are general registers if RF function is disabled. When PW1_E (PW2_E) = 1, a continuous pulse train is generated to P92 (P93).

Example: When PW1_E (PW2_E) = 1 and Timing Rate = 1 : 1. The High level signal time is defined by R10 (R11) μ S. And the Low level signal time = 255-R10 (R11) μ S. If R10 (R11) = 0, P92 (P93) all in low. If R10 (R11) = 0xFF, P92 (P93) all in high.

R10: high level time of the 1st PWM module that outputs to P92.

R11: high level time of the 2nd PWM module that outputs to P93.

7.2 Special Purpose Registers

7.2.1 A (Accumulator)

Internal data transfer, or instruction operand holding. It is not an addressable register.

7.2.2 CONT (Control Register): default (0b0011_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
S7	INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

Bit 0 (PSR0) ~ Bit 2 (PSR2): WDT pre-scalar bits. WDT's time base = ?

Bit 3 (TSR0) ~ Bit 5 (TSR2): TCC prescaler bits

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 6 (INT) Interrupt enable flag which cannot be written by CONTW instruction.

- 0: interrupt masked by DISI
- 1: interrupt enabled by ENI/RETI instruction

Bit 7 (S7): P76/P77 LED driving ability bit

- 0: disable LED driving ability function
- 1: enable driving ability function

Bits 0~5, 7 of CONT register are readable and writable.

7.2.3 IOC5 ~ IOC9 (I/O Port Control Register): default (0b1111_1111)

- "0" put the relative I/O pin as output
- "1" put the relative I/O pin into high impedance
- IOC5 ~ IOC9 are five I/O direction control registers.

7.2.4 IOCA (PS/2 USB Control Register): default (0b1100_0000)

Bit 7 ~ Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOW FREQ. switch	/P76_7 Pull-up	Remote WakeUp Status	ExtRAM_S	RF function	PS/2	USB

Bits 1, 0 (PS/2 enable, USB enable): PS/2 or USB enable bit

- 00: Default situation. Pull high 200 kΩ on P74 and P75.
- 01: Enable USB function. Pull high 1.5k ohm on P75 (D-).
- 10: Enable PS/2 function, enable wake up function and pull high 4.7KΩ on P74~P77. P74~P75 are pulled high by Transceiver.
- 11: Test mode for P74~P77. P74~P77 will not be pulled up any resistor.

Bit 2 (RF Function): RF receive function enable bit. If RF function is disabled, R10~R13 & P92~P93 functions normally. Before user sets the RF Timing counter (R10~R13), user has to enable the RF function bit (set this bit = 1). RF functions as follows:

- a. R10~R13: RF Timing counter
- b. P92, P93: RF receives pins
- 0: disable RF function
- 1: enable RF function

Bit 3 (ExtRAM_S): Select the register segment. After selecting the segment of register, the data of RA~RE and ERA~ERE can not be changed. The registers of RA~RE and ERA~ERE are independent.

- 0: RA~RE selected
- 1: ERA~ERE selected
- ERA~ERE are described in Section 7.3 Extra Registers.



Bit 4 (Remote Wake-up Status): Indicates whether the device is currently requested to support remote wakeup or not. The Remote Wake-up field can be modified by SetFeature() and ClearFeature() requests.

- 0: does Not support Remote wake up
- 1: supports Remote wake up

Bit 5 (/P76_7 Pull-up) P76/P77 Pull-up enable bit in USB Mode

- 0: enable Pull-up
- 1: disable Pull-up

Bits 6, 7 (Low Freq. switch): Low frequency switches. The range of the frequency is between +-30%.

- 00: Frequency: 500 Hz
- 01: Frequency: 4 kHz
- 10: Frequency: 32 kHz
- 11: Frequency: 256 kHz

7.2.5 IOCB (Port 9 Wake-up Control): default (0b1111_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/P96	/P95	/P94	/P93	/P92	/P91	/P90

Bits 0~6 (/P90~/P96): Control bit used to enable the wake-up function of P90~P96.

- 0: enable wake-up function
 - 1: disable wake-up function
- All bits are readable & writable.

Bit 7: Not used.

7.2.6 IOCC (Port 9 LED Driving Ability): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P96	P95	-	P93	P92	P91	P90

Bits 0~3, 5~6 (P90~P93, P95~P96) Control bit used to enable the LED driving ability of P90~P93, P95~P96.

- 0: disable LED driving ability function
 - 1: enable driving ability function
- All bits are readable & writable.

Bit 4 and Bit 7: Not used.

7.2.7 IOCD (Port 9 Pull-high Control Register): default (0b1111_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/P96	/P95	-	/P93	/P92	/P91	/P90

Bits 0~3, 5~6 (/P90~/P93,/P95~/P96): Control bit used to enable pull-high function of P90~P93, P95~P96. All bits are readable & writable.

0: enable pull-high function

1: disable pull-high function

Bit 7 Not used.

7.2.8 IOCE (Pull-high Control Register & WDT Control Register): default (0b1101_0111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/LOW FREQ.	/WUE	WTE	SLPC	Dev_Resume	/PU8	/PU6	/PU5

Bits 0~2 (/PU5~/PU8: Pull-High Control Register): Default = 1, Disable pull high.

P74~P77 are pulled-high by IOCA setting.

0: enable pull-high function

1: disable pull-high function

Bit 3 (Dev_Resume): DEV_RESUME control bit. To set DEV_RESUME = 1 to UDC, reset DEV_RESUEM = 0 by hardware. This bit is readable and writable.

Bit 4 (SLPC) This bit is set by hardware at the falling edge of the wake-up signal and is cleared by software. SLPC is used to control the operation of the oscillator. The oscillator is disabled (oscillator is stopped, the controller enters the Sleep 2 Mode) on high-to-low transition of the SLPC bit and is enabled (the controller is awakened from Sleep 2 Mode) on low-to-high transition of the SLPC bit. In order to ensure the stable output of the oscillator, once the oscillator is disabled and is enabled again, there should be a delay by OST (Oscillator Start-up Timer) of MTP code option, before the next program instruction is being executed. The OST is always activated by wake-up from sleep mode.

Bit 5 (WTE): Control bit used to enable the Watchdog Timer. WTE bit is readable and writable.

0: disable WDT

1: enable WDT

Bit 6 (/WUE) Control bit used to enable the wake-up function of P60~P67, P74~P77 (Port change wakeup). /WUE bit is readable and writable.

0: enable wake-up function

1: disable wake-up function

P74~P75 in USB mode has no wake-up function. Note: D+/D- wakes up the UDC first.



Bit 7(/Low Freq.): Dual Clock Control bit. This bit is used to select the frequency of system clock. When this bit is set to 0, the MCU will run on very slow frequency for power saving and the UDC will stop working.

- 0: Slow frequency (500Hz~256 kHz)
- 1: Normal frequency

7.2.9 IOCF (Interrupt Mask Register): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Resume_IE	RF2_IE	RF1_IE	P74/P75/P76/ P77_IE	USBReset_IE	Suspend_IE	EP0_IE	TCIE

Bit 0 (TCIE): TCIF interrupt enable bit

- 0: disable TCIF interrupt
- 1: enable TCIF interrupt

Bit 1 (EP0_IE): UDC interrupt enable bit

- 0: disable UDC interrupt
- 1: enable UDC interrupt

Bit 2 (Suspend_IE): UDC suspend interrupt enable bit

- 0: disable UDC suspend interrupt
- 1: enable UDC suspend interrupt

Bit 3 (USBReset_IE): USB reset interrupt enable bit

- 0: disable USB reset interrupt
- 1: enable USB reset interrupt

Bit 4 (P74/P75/P76/P77_IE): P74, P75, P76, P77 voltage level change interrupt enable bit. But it only has P76/P77 voltage level change interrupt function in USB mode.

- 0: disable P74, P75, (P76, P77) voltage level change interrupt
- 1: enable P74, P75, (P76, P77) voltage level change interrupt

Bit 5 (RF1_IE): RF1 Timing counter interrupt enable bit. The condition is described in RF Timing counter function below.

Bit 6 (RF2_IE): RF2 Timing counter interrupt enable bit. The condition is described in RF Timing counter function below.

Bit 7 (Resume_IE): Host resume interrupt enable bit in Low Freq. mode. The program is interrupted when the PC resumes operation of the device, if this bit is set. When the PC resumes operation of the device, the UDC will de-assert UDC_SUSPEND to MCU. If UDC_SUSPEND is de-asserted by DEV_RESUME, it will not cause any interrupt.

Individual interrupt is enabled by setting its associated control bit in IOCF to "1".

The IOCF Register is readable and writable.

7.3 Extra Registers

7.3.1 ERA (AD Controller/AD Selection Pin): default (0b0001_1111)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD_start	-	-	AD_A4	AD_A3	AD_A2	AD_A1	AD_A0

Bits 4~0 (AD_A4~AD_A0): AD number. If the AD number is from zero to 0¹⁷, the AD converter will be powered on. Otherwise, power off.

00000: Disable AD function & power off the AD converter

AD number	00000	00001	00010	00011
AD pin	AD0	AD1	AD2	AD3
AD number	00100	00101	00110	00111
AD pin	AD4	AD5	AD6	AD7
AD number	01000	01001	01010	01011
AD pin	AD8	AD9	AD10	AD11
AD number	01100	01101	01110	01111
AD pin	AD12	AD13	AD14	AD15
AD number	10000	10001	10010	10011
AD pin	AD16	AD17	AD18	AD19
AD number	10100	10101	10110	10111
AD pin	AD20	AD21	AD22	AD23

Bit 7 (AD_start): Converted Analog to Digital start. If AD_start is set to 1 by software, the AD converter will start converting. It is reset by hardware when conversion from Analog to Digital is completed.

7.3.2 ERB, ERC (AD input DATA): AD input data for selecting pin. Default (0b0000_0000). Read Only

ERC (7~0)	ERB (7~6)	ERB (5~0)
Bit 9~Bit 2	Bit 1~Bit 0	-

When the A/D conversion is completed, the result is loaded to ERB & ERC.

7.3.3 ERD (AD Conversion Rate): default (0b0000_0000)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	USB_Token	AD_R1	AD_R0

Bits 1~0 (AD_R1~AD_R0): AD conversion rate

00: 256K

01: 128K

10: 64K

11: 32K

Bit 2 (USB_Token): Set when USB Token from Host. Reset by software.

7.3.4 ERE (PWM_CNT): default (0b0000_0001)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PW2_E	PW1_E	-	-	-	PWM_SR2	PWM_SR1	PWM_SR0

Bit 2 (PWM_SR2) ~ Bit 0 (PWM_SR0): PWM pre-scaler bits.

In 6 & 12 MHz

PWM_SR2	PWM_SR1	PWM_SR0	Timing Rate	Time of High Period
0	0	0	1:1/2	0.5 μ s (127.5 μ s)
0	0	1	1:1	1 μ s (255 μ s)
0	1	0	1:2	2 μ s (510 μ s)
0	1	1	1:4	4 μ s (1020 μ s)
1	0	0	1:8	8 μ s (2.04ms)
1	0	1	1:16	16 μ s (4.08ms)
1	1	0	1:32	32 μ s (8.16ms)
1	1	1	1:64	64 μ s (16.32ms)

Bit 6 (PW1_E): The 1st PWM module enable bit

0: Disable the PWM function of the 1st module

1: Enable the PWM function of the 1st module

Bit 7 (PW2_E): The 2nd PWM module enable bit

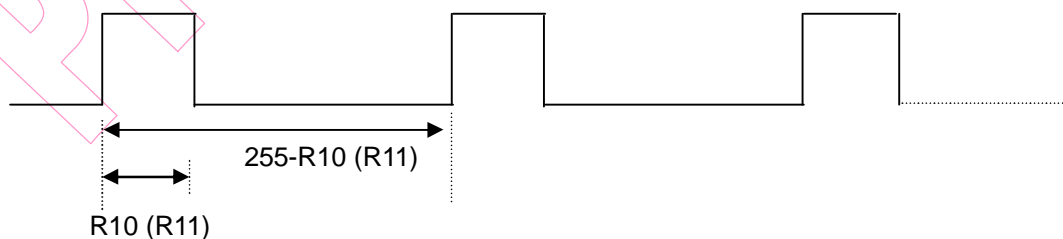
0: Disable the PWM function of the 2nd module

1: Enable the PWM function of the 2nd module

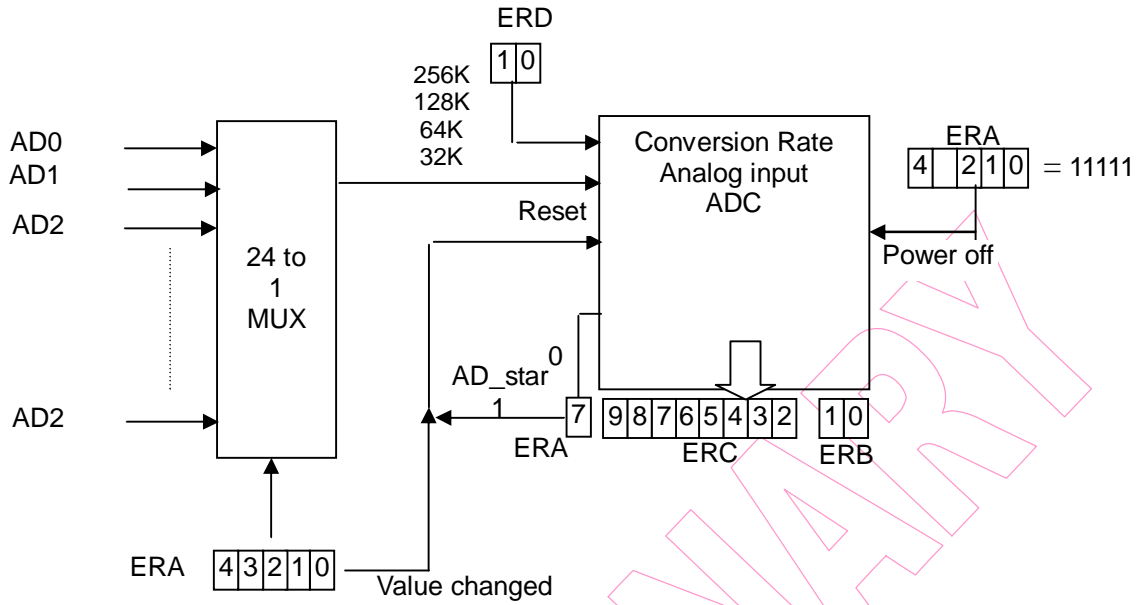
PWM Example:

When PW1_E (PW2_E) = 1 and Timing Rate = 1 : 1, a continuous pulse train is generated to P92 (P93). The signal is high first then low. Its pulse time-out period is 255 μ s. The High level signal time is defined by R10 (R11) μ s. And the Low level signal time = 255-R10 (R11) μ s. The continuous pulse is stopped after PW1_E (PW2_E) = 0. If R10 (R11) = 0, P92 (P93) are all in low. If R10 (R11) = 0xFF, P92 (P93) are all in high.

Timing:



7.4 Analog to Digital Converter (ADC)



EEPROM process:

1. Save value to Register
2. Program
3. Read
4. Polling EE_O.K

7.5 Sleep and Wake up

The EM78M611E supports three kinds of saving power mode.

- (1) Sleep 1 mode
- (2) Sleep 2 mode
- (3) Low Freq. Mode

The Sleep 1 Mode (power-down mode) can be entered by executing SLEP instruction. While entering Sleep 1 Mode, the WDT (if enabled) is cleared but keeps running. The controller can be awakened by WDT timeout (if enabled), and it will cause the controller to be reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

The Sleep 2 Mode is caused by clearing “SLPC” bit of the IOCE register. **Before entering Sleep 2 Mode in USB application, hardware has to check UDC_SUSPEND = 1. IF not, the MCU will not enter Sleep 2 Mode.** In this mode, the controller can be awakened by the following conditions:

- (A) Port (P60~P67, P74~P77, P90~P97) change wake-up. When wake-up, the controller will continue to execute program in-line. In this case, before entering Sleep 2 Mode, the wake-up function of the trigger sources (P60~P67, P74~P77, or P90~P97) should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noted is that after waking up, the WDT is enabled. The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

In USB mode, it has to trigger the DEV_RESUME to UDC after waking up.

- (B) The PC resumes device operation in USB mode. In this case, the UDC will fall down the UDC_SUSPEND, the MCU would wake-up in reset time.

Sometime noise enters D- or D+, and UDC will cause UDC_SUSPEND down. But it is not Host Resume condition, so the MCU cannot be awakened at this time.

Hardware delays for 100 ns during this situation.

- (C) WDT time-out (if enabled). When wake-up, will cause a controller reset.

The Low Freq. mode is caused by clearing “Low Freq.” bit of the IOCE register. After clearing this bit, the MCU runs in low frequency (about 500Hz ~ 256kHz). The controller can run in normal frequency by setting this bit. It has no I/O wake-up function in this mode.

7.6 MTP Mode Description

7.6.1 MTP Pin Definition

Symbol	Port	Type	Function
VPP	P94	I	Programming voltage input. Vpp is 10V
VNN	VNN	I	-10V
OSCI	OSCI	I	CLK for OTP memory address increment
DATAIO	P56	I/O	ROM code DATA input & output pin
DINCK	P57	I	ROM code CLK input & output pin
/PGM	P55	I	Program write enable. Active low.
/OE	P54	I	Output enables. Active low.

7.6.2 Option Mode

Bits 12~4	Bits 3~2	Bit 1	Bit 0
User ID	OST	Frequency Selection	/PT

Bit 25	Bit 24	Bits 23~21	Bit 20	Bit 19	Bit 18	Bit 17	Bits 16~15	Bits 14~13
Not Used	UDC Response	EP2 Max Size	EP2 Direction	EP2 Enable	/AD_HOLD	/R.S.	Not Used	Pack Sel

Bit 0: Protect bit

- 0: Enable
- 1: Disable

Bit 1: Frequency Selection

- 0: MCU runs on 12MHz
- 1: MCU runs on 6MHz

Bits 3~2: OST: Oscillator Start-up Timer

- 00: 500 μ s
- 01: 2 mS
- 10: 8 mS
- 11: 16 mS

Bits 12~4: User ID. Defined by user when written to

Bits 14~13: Package type selector

- 00: Not defined
- 01: 40 pins
- 10: Not defined
- 11: 44 pins

Bits 16~15: Not Used

- Bit 17:** R.S. Transceiver enable
- 0: enable Resistor Switch
 - 1: disable Resistor Switch
- Bit 18:** Hold MCU when AD convert
- 0: hold MCU when AD converts
 - 1: keep run MCU when AD convert
- Bit 19:** EP2 Enable
- 0: Disable
 - 1: Enable
- Bit 20:** EP2 Direction
- 0: Output
 - 1: Input
- Bit 23~21:** EP2 max. size
- 111 ~ 000: 8~1 Bytes
- Bit 25~24: Bits 16~15:** Not Used

7.7 Product Module

Code Option	Bits 14~13 (Pack sel.)	Description
EM78M611EXAAP	01	40 pins DIP+ Normal function
EM78M611EXDAP	01	40 pins DIP+ EEPROM + AD
EM78M611EXAAQ	11	44 pins QFP+ Normal function
EM78M611EXDAQ	11	44 pins QFP+ EEPROM + AD
EM78M611EXABP	11	20 pins DIP+ Normal function
EM78M611EXDBP	11	20 pins DIP+ EEPROM + AD
EM78M611EXABM	11	20 pins SOP+ Normal function
EM78M611EXDBM	11	20 pins SOP+ EEPROM + AD
EM78M611EXADM	11	20 pins SSOP+ Normal function
EM78M611EXDDM	11	20 pins SSOP+ EEPROM + AD
EM78M611EXACP	11	24 pins DIP+ Normal function
EM78M611EXDCP	11	24 pins DIP+ EEPROM + AD
EM78M611EXACM	11	24 pins SOP+ Normal function
EM78M611EXDCM	11	24 pins SOP+ EEPROM + AD



8 DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IIL	Input Leakage Current	VIN = VDD, VSS			±1	μA
VIH	Input High Voltage		2.0			V
VIL	Input Low Voltage				0.8	V
VIHX	Clock Input High Voltage	OSCI	2.5			V
VILX	Clock Input Low Voltage	OSCI			1.0	V
VOH1	Output High Voltage (P70~P72, P76, P77)	IOH = -10.0mA VDD = 5V		2.4		V
VOH2	Output High Voltage (P74, P75)	IOH = -5.0mA VDD = 5V		2.4		V
VOH3	Output High Voltage (Ports 5, 6, 8, P90~P93, P95, P96)	IOH = -10.0mA Vreg = 3.3V		2.4		V
VOL1	Output Low Voltage (P76~77 : Normal Mode)	IOL = 10.0mA VDD = 5V		0.4		V
VOL2	Output Low Voltage (P74~P75)	IOL = 5.0mA VDD = 5V		0.4		V
VOL3	Output Low Voltage (P70~P72, P76~P77 : LED driver Mode)	IOL = 10.0mA VDD = 5V		3		V
VOL4	Output Low Voltage (Port 5,6,8) (P90~P96 : Normal Mode)	IOL = 10.0mA Vreg = 3.3V		0.4		V
VOL5	Output Low Voltage (P90~P96 : LED driver Mode)	IOL = 10.0mA Vreg = 3.3V		1		V
IPH1	Pull-high current (Ports 5, 6, 8, P90~P93, P95, P96)	Pull-high active, input pin at VSS (PH resistor = 25kΩ), Vreg=3.3V		-125		μA
IPH2	Pull-high current (P74~P77)	Pull-high active, input pin at VSS (PH resistor = 2.2kΩ)		2.27		mA
IPH3	Pull-high current (P75 in USB mode)	Pull-high active, input pin at VSS (PH resistor = 1.5kΩ)		2.2		mA
ISB1	Power-down current	All input and I/O pin at VDD, Output pin floating, WDT disabled			50	μA
ISB2	Power-down current	All input and I/O pin at VDD, Output pin floating, WDT enabled			100	μA
ICC1	Operating supply current	Fosc= 6.0 MHz , Output pin floating			10	mA
ICC2	Operating supply current	Fosc= 12.0 MHz, Output pin floating			20	mA
ICC3	Operating supply current	Fosc= 256 kHz, Output pin floating			200	uA
Vreg	Output Voltage of Internal		3.0		3.6	V
Vresetl	Low Power Reset detection low voltage				2.2	V
Vreseth	Low Power Reset detection high voltage		3.0			V

9 Application Circuit

