

Compal Confidential

M/B Schematics Document

Intel Skylake-H 4+2+ AMD Tropo XT2

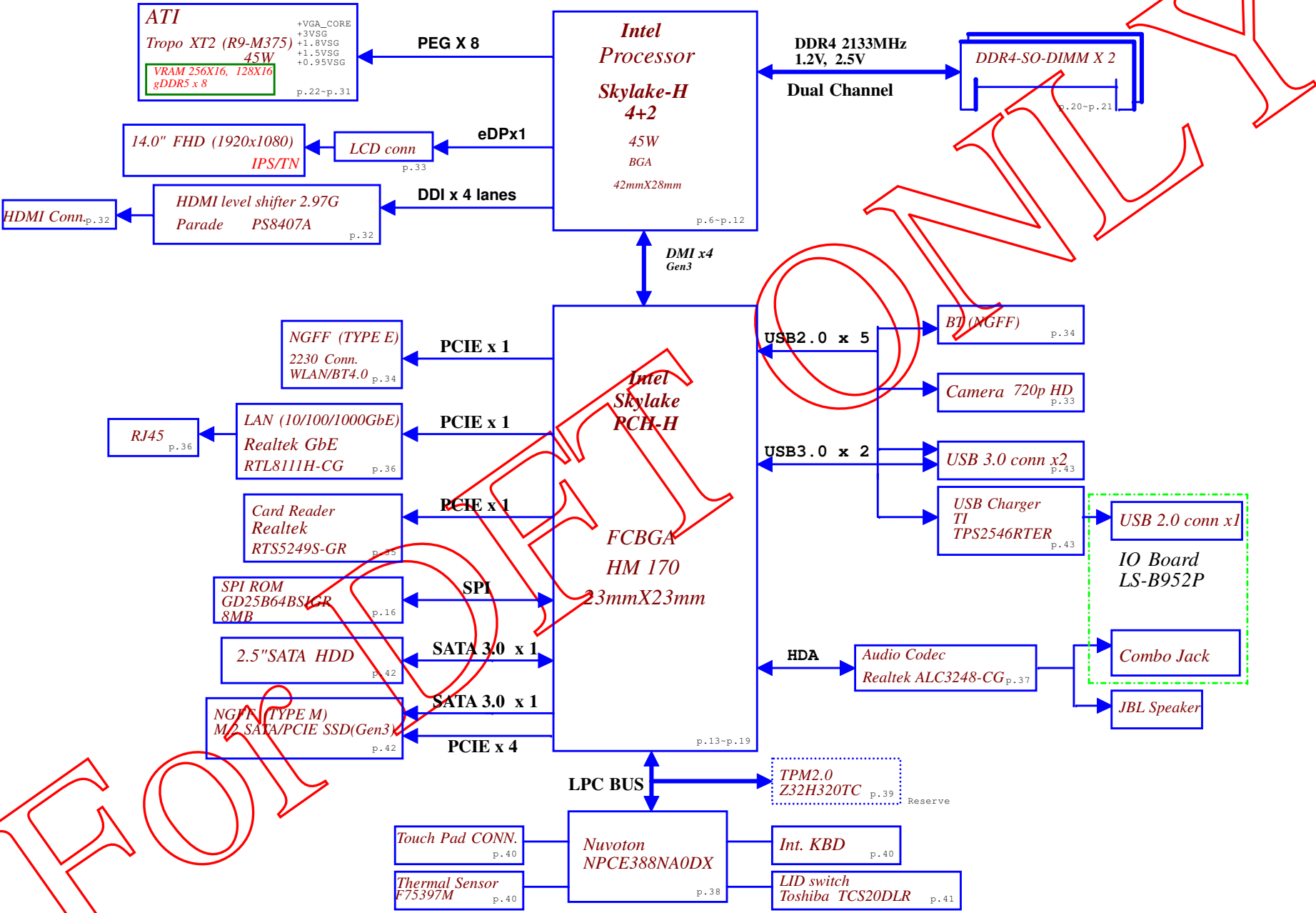
LA-C951P

2015-08-14

REV:1.0

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Skylake-H



BOM Structure Table

Function	Stuff	Un-Stuff
DGPU SKU	DIS@	@DIS@
SPI_I03(MOW36)	QS@	ES@
2G VRAM	V2G@	
4G VRAM	V4G@	
NC Components		@
CMC		CMC@
TPM		TPM@
EMI	EMI@	@EMI@
ESD	ESD@	@ESD@
RF	RF@	@RF@
ISCT	NOISCT@	ISCT@
MPHY_EXT	NOEXTMPHY@	EXTMPHY@
CPU	CPU5@/CPU6@	
KB ID	NOKBL@/KBL@	

HSIO Port Table

HSIO Port	Capable	Device	PCIE CLK	NOTE
1	USB3.0_1 / OTG	NA		
2	USB3.0_2 / SSIC_1	NA		
3	USB3.0_3 / SSIC_2	USB3.0 (MB_UP)		
4	USB3.0_4	USB3.0 (MB_DOWN)		
5	USB3.0_5 / PCIE_1	NA		
....	
12	PCIE_6	WLAN(NGFF_KEY E)	CLK3	
....	
16	PCIE_10 / SATA_1A	HDD_SATA		
17	PCIE_11	Card Reader	CLK2	
18	PCIE_12	LAN	CLK1	
19	PCIE_13 / SATA_0B	SSD_SATA	CLK4	Opt i on SS D t y p e
20	PCIE_14 / SATA_1B	SSD_PCle x 4		
21	PCIE_15 / SATA_2			
22	PCIE_16 / SATA_3			
....	

USB2.0 Port Table

USB2.0 Port	Device
1	USB3.0 (MB_UP)
2	USB3.0 (MB_DOWN)
3	NA
4	BT (NGFF)
5	NA
6	USB2.0 (IO_Charge Port)
7	NA
8	Camera
9	NA
10	NA

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA0
		DIMM2	TBC	TBC	0xA4
		TP	TBC	TBC	TBC
SML0CLK SML0DATA	+3VS		TBC	TBC	TBC
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		Thermal sensor	1001100	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBUS Port 1	+3VLP	BAT	TBC	TBC	TBC
		CHGR	TBC	TBC	TBC
SMBUS Port 2	+3VLP	TP (reserve)	TBC	TBC	TBC
	+3VLP	Thermal sensor	1001100	TBC	TBC

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft t Off)		LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

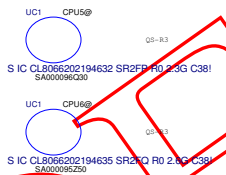
Power Plane	Description	S0	S3	S4/S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power drcut	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCSTG	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available otherwise it is OFF

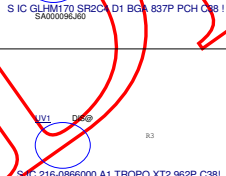
Load BOM Opt i on Table

BOM Number	Load BOM Opt i on
4519YS38L09	DIS@/QS@/EMI@/ESD@/RF@/NOEXTMPHY@/HM170@/NOISCT@/CPU5@/KBL@
4519YS38L12	DIS@/QS@/EMI@/ESD@/RF@/NOEXTMPHY@/HM170@/NOISCT@/CPU6@/KBL@

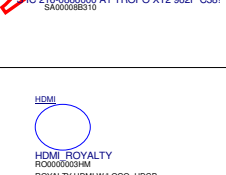
CPU/PCH part



PCH-H



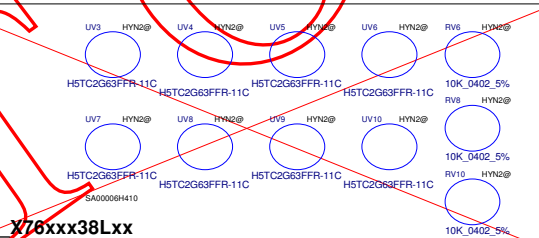
VGA



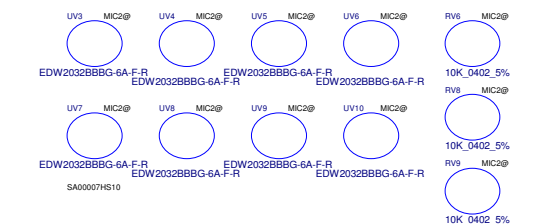
HDMI



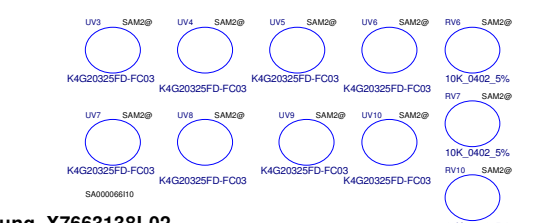
2G X7663138L01



Hynix_X76xxx38Lxx

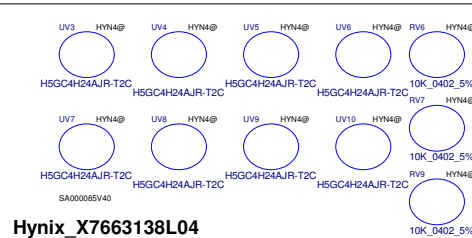


Micron_X7663138L01

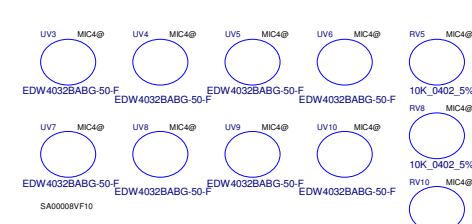


Samsung_X7663138L02

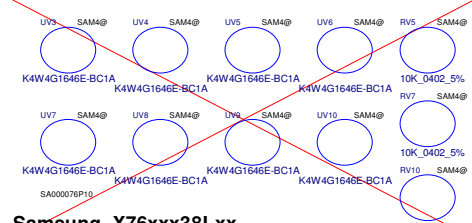
4G X7663138L03



Hynix_X7663138L04



Micron_X7663138L03



Samsung_X76xxx38Lxx



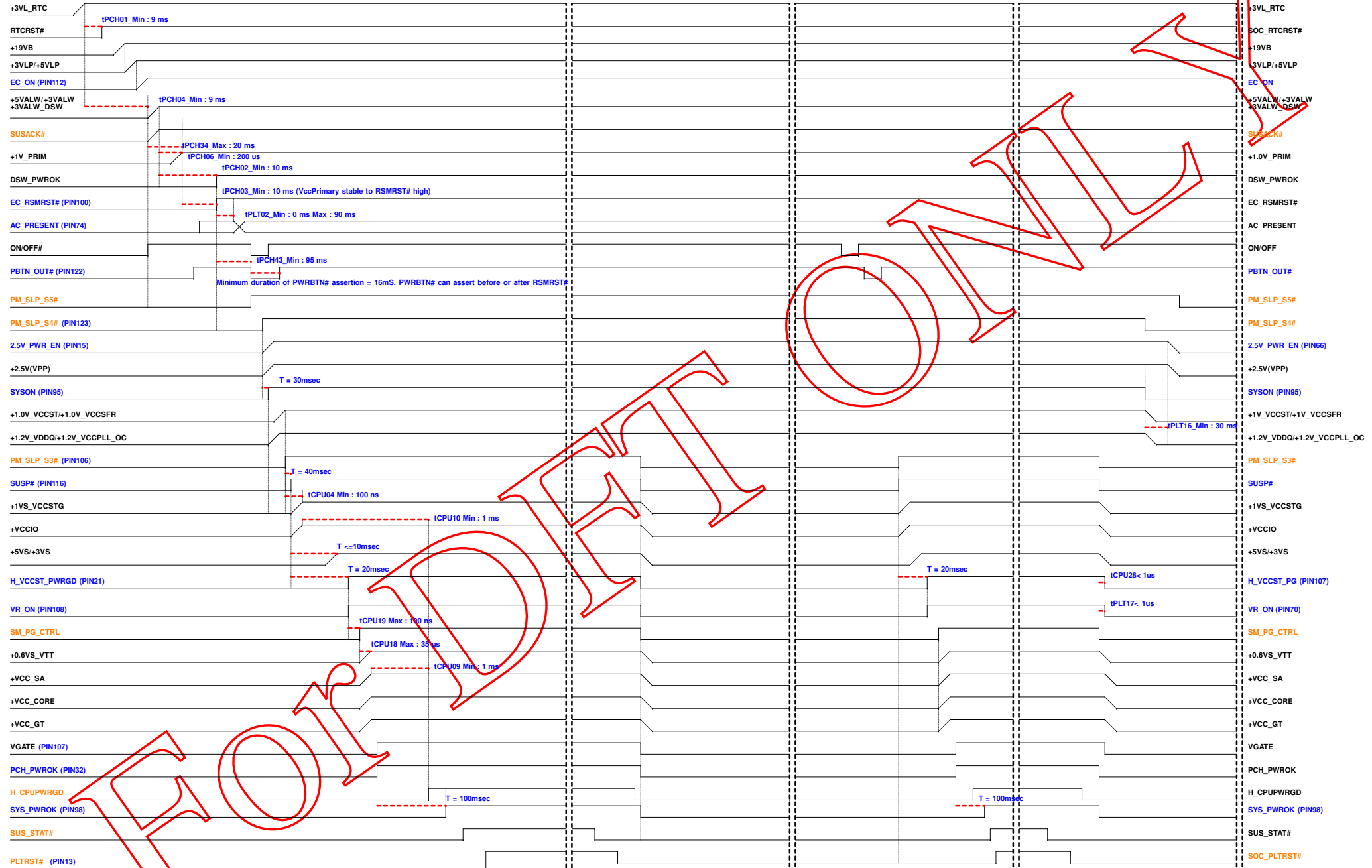
For

G3→S0

S0→S3

S3 →S0

S0→S5





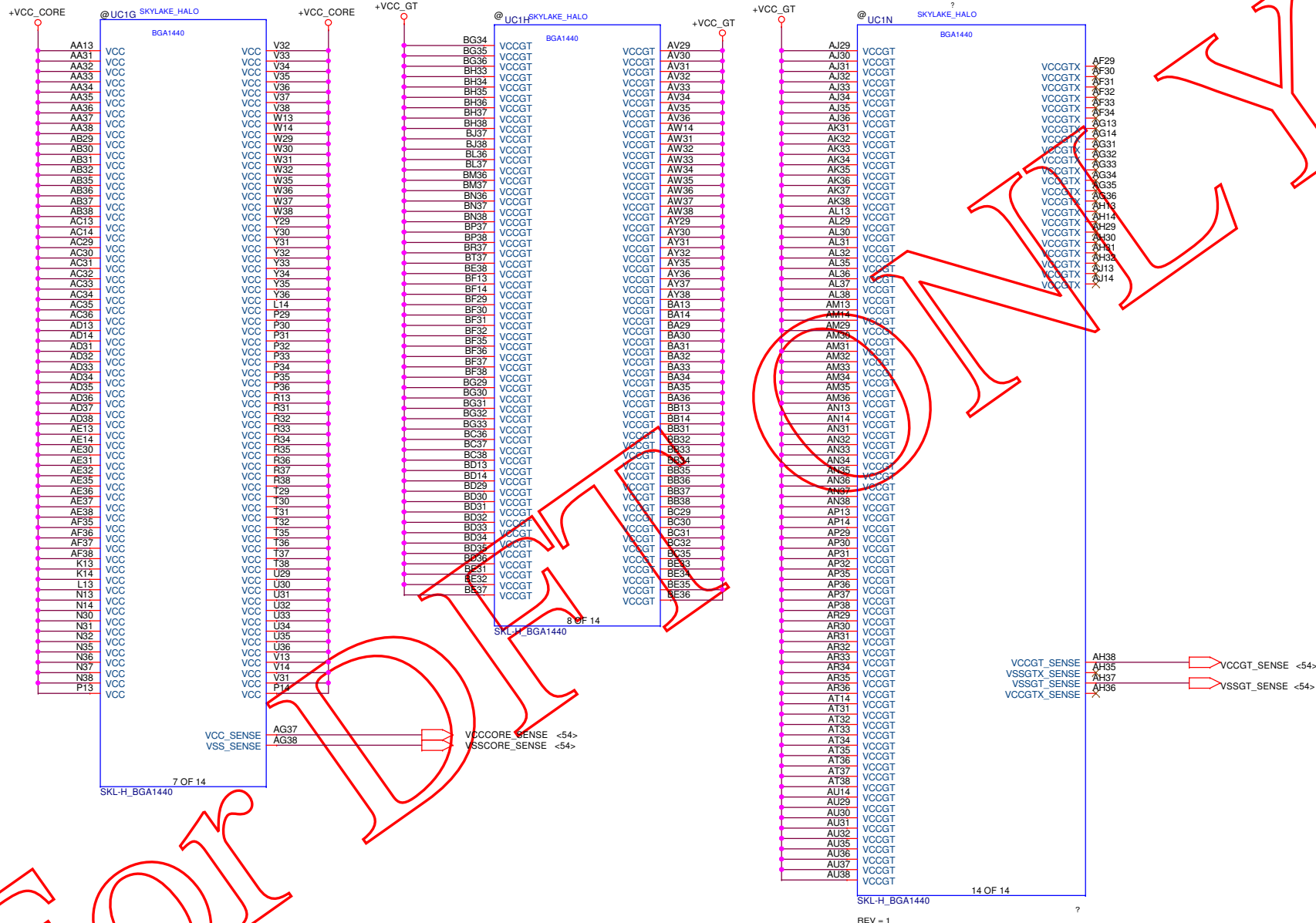
+VCCIO
RC7 1 24.9_0402_1%
2
PEG_RCOMP

Note:
Trace width=12 mils,Spacing=15mils
Max length= 400 mils.

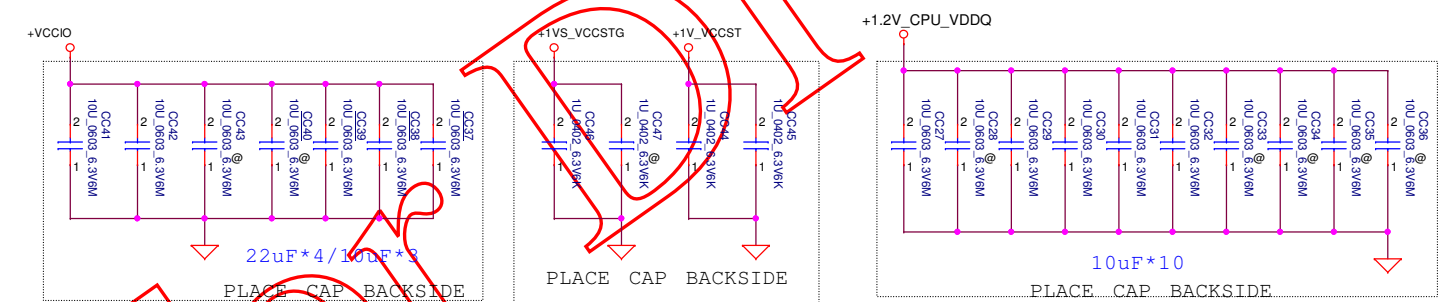
+VCCIO
RC8 1 24.9_0402_1%
2
EDP_COMP

Note:
Trace width=20 mils,Spacing=25mils
Max length= 100 mils.

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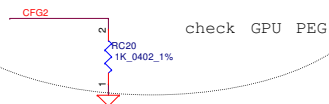


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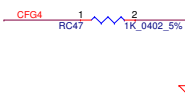


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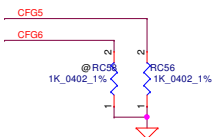
CFG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed



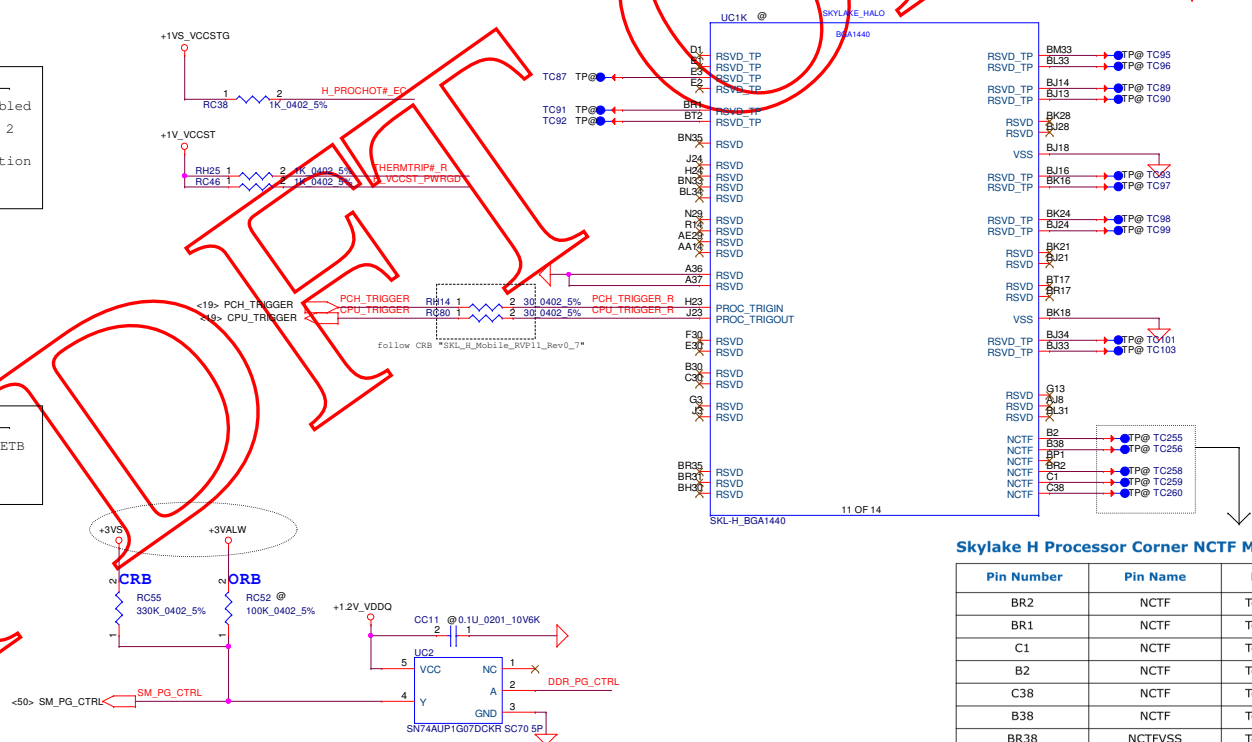
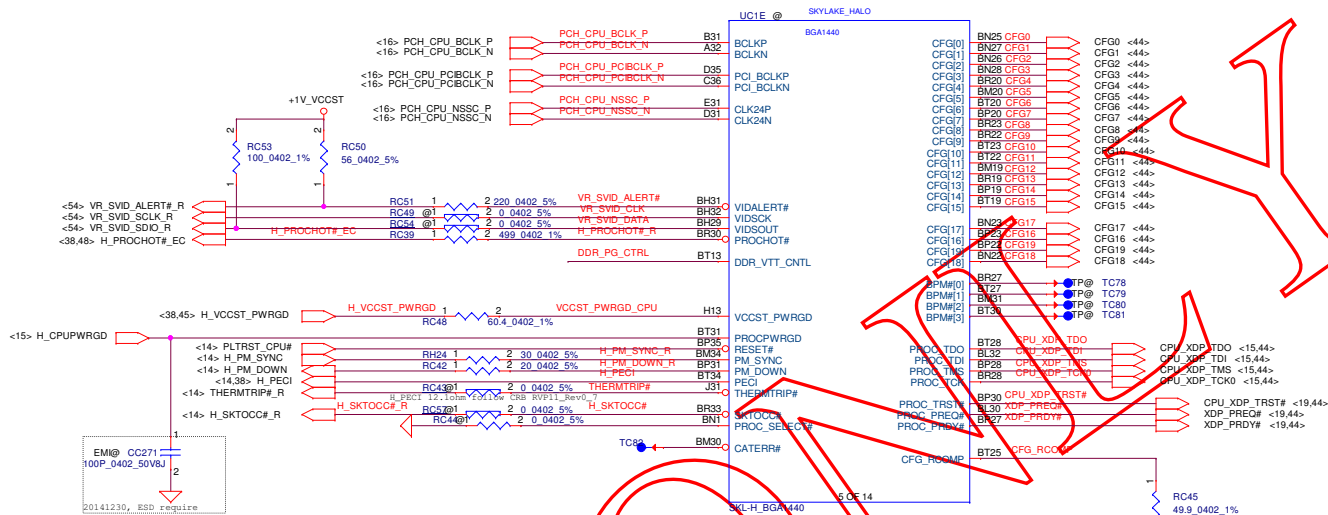
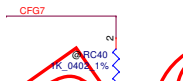
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



```
CFG[6:5] 11: (Default) x16 - Device 1 functions 1 and 2 disabled
          *10: x8, x8 - Device 1 function 1 enabled ; function 2
              disabled
          01: Reserved - (Device 1 function 1 disabled ; function
              2 enabled)
          00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

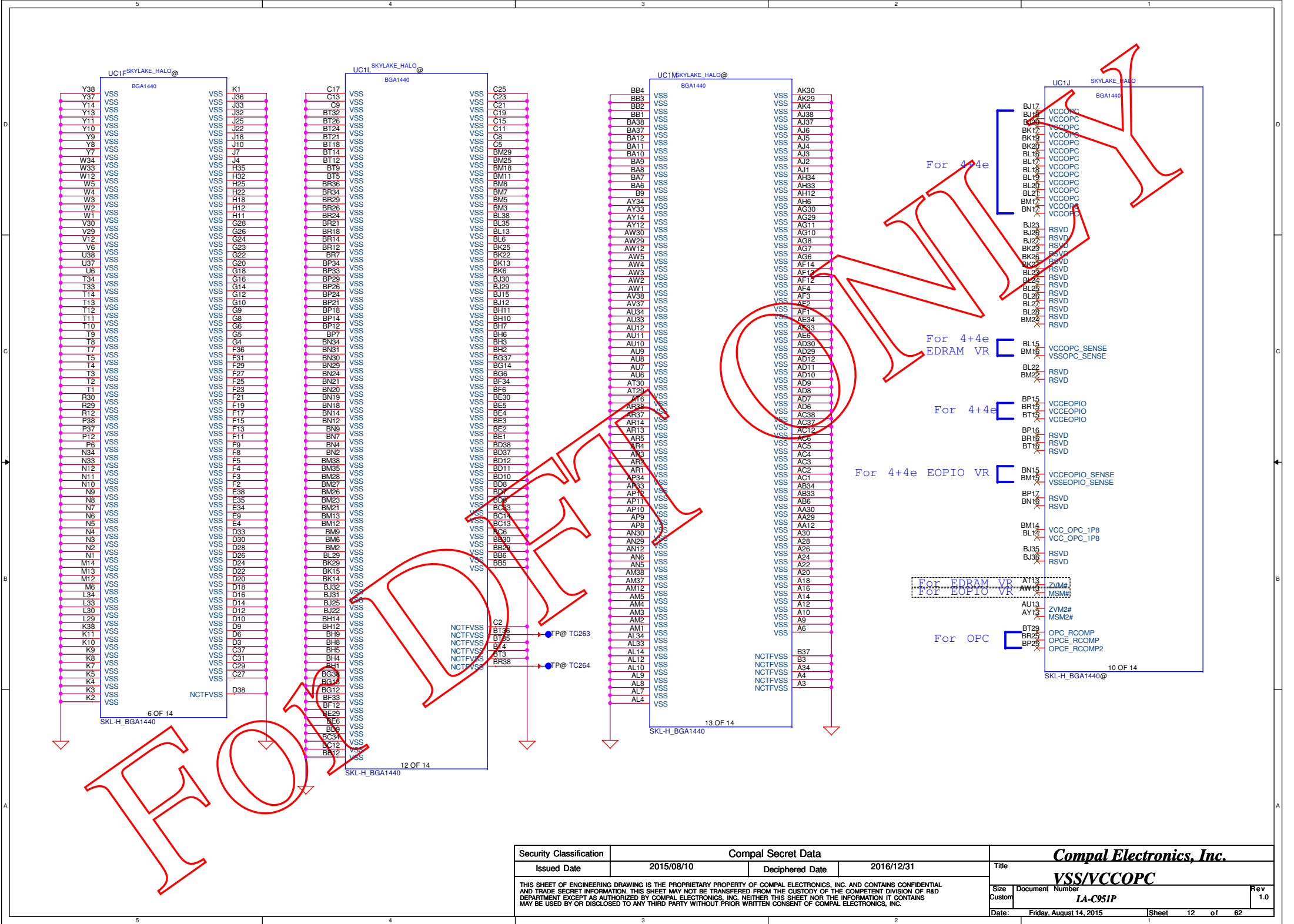


CFG7	<p>* 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
------	--



Pin Number	Pin Name	Description	Corner
BR2	NCTF	Test Point (TP)	Corner BT1
BR1	NCTF	Test Point (TP)	
C1	NCTF	Test Point (TP)	Corner A1
B2	NCTF	Test Point (TP)	
C38	NCTF	Test Point (TP)	Corner A38
B38	NCTF	Test Point (TP)	
BR38	NCTFVSS	Test Point (TP)	Corner BT38
BT36	NCTFVSS	Test Point (TP)	

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For 4+4e

For 4+4e
EDRAM VR

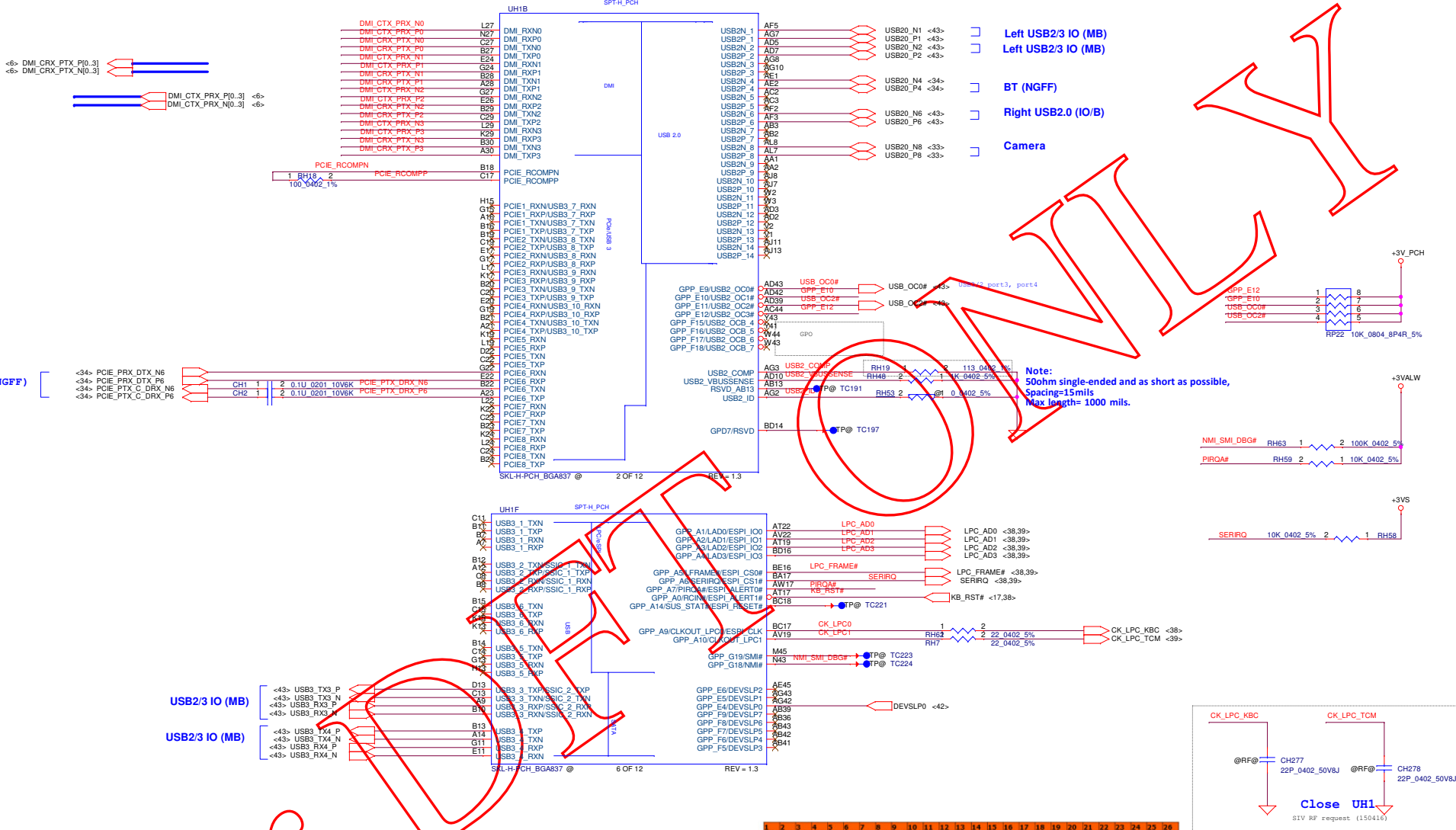
For 4+4e

For 4+4e EOPIO VR

For EDRAM VR
For EOPIO VR

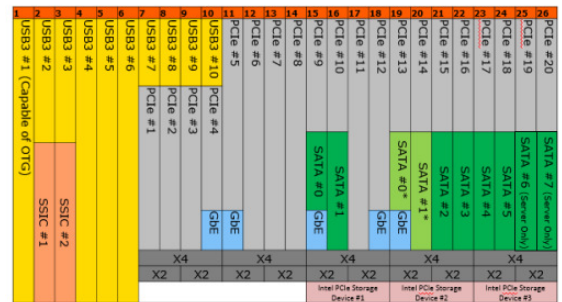
For OPC

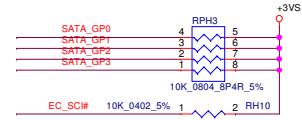
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USB2.0							
Port	1	2	3	4	5	6	7
	Left USB3.0	Left USB3.0				Right USB2.0	Camera

Flexible I/O Capable Ports							
HSIO Port	3	4	5	6	7	8	9
USB 3.0	USB3.0_1	USB3.0_2					
PCIe							
SATA							





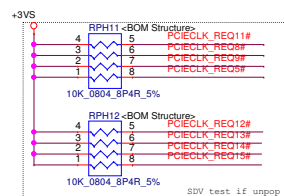
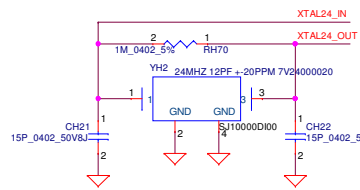
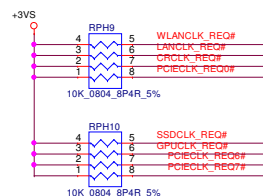
SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0 OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe / LAN	PCIe	PCIe	PCIe
H170	USB 3.0 OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe	PCIe / LAN	PCIe / LAN	PCIe	PCIe	PCIe
HM170	USB 3.0 OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0 / PCIe	USB 3.0 / PCIe	PCIe	PCIe / LAN	PCIe / LAN	PCIe	PCIe	PCIe

SKU	15	16	17	18	19	20	21	22	23	24	25	26
H110	PCIe/LAN	PCIe	N/A	LAN Only	SATA/LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A
H170	PCIe/LAN /SATA	PCIe*/SATA	PCIe	PCIe/LAN	PCIe/LAN /SATA	PCIe*/SATA	PCIe*/SATA	PCIe*/SATA	SATA	SATA	PCIe	PCIe
HM170	PCIe/LAN /SATA0	PCIe*/LAN/ SATA1	PCIe	PCIe/LAN	PCIe*/LAN/ SATA0	PCIe*/SATA1	PCIe*/SATA	PCIe*/SATA	N/A	N/A	N/A	N/A

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect

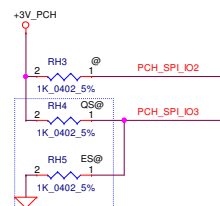
Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

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								SATA,GPIO					
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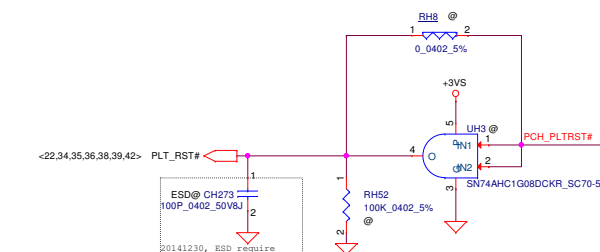
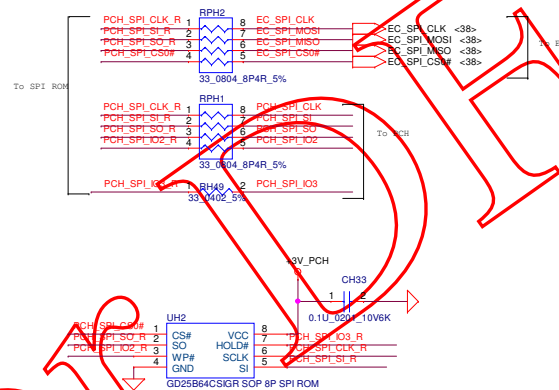
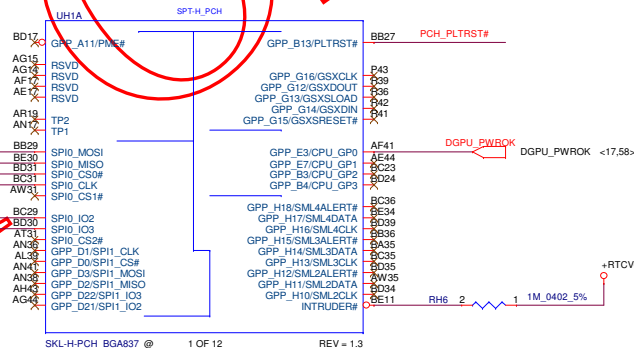
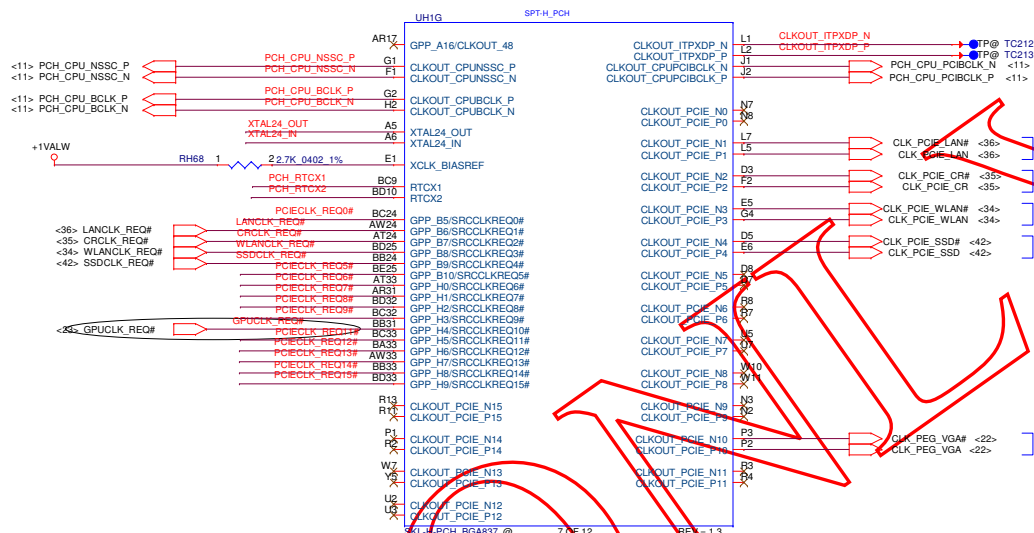


<44> XDP_SPI_SI RH1 1 2 1K 0402 1% PCH_SPI_SI
<44> XDP_SPI_IO2 RH2 1 CMC@ 2 1K 0402 1% PCH_SPI_IO2

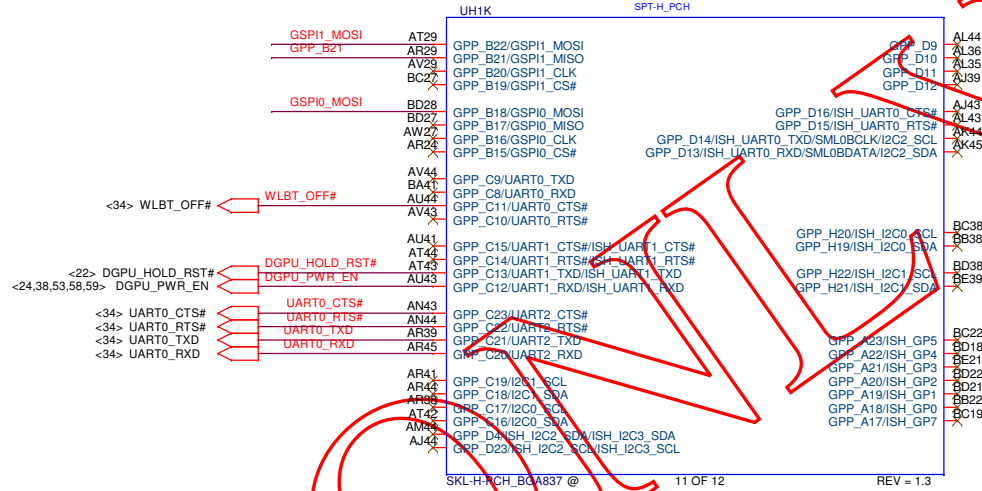
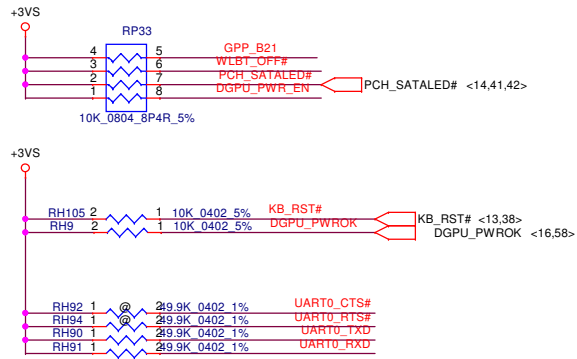
RH45/46 place to within 1100 mil of SPI0 MOSI/SPI0 IO2 pin for XDP



PCH STRAPS
PERSONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



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Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

- 0 = Disable TOP Swap mode.--> ORB Use
- * 1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

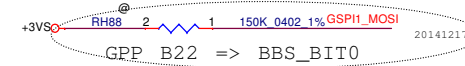
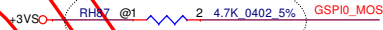
No Reboot

- * 0 = Disable No Reboot mode. --> ORB Use
- 1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

- *0 = SPI Mode --> ORB Use
- 1 = LPC Mode

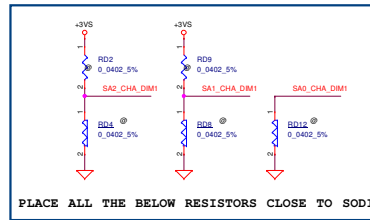


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				LA-C951P	
				Date:	Friday, August 14, 2015
				Sheet	17 of 62

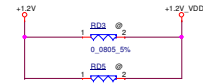
CHANNEL-A

Interleaved Memory

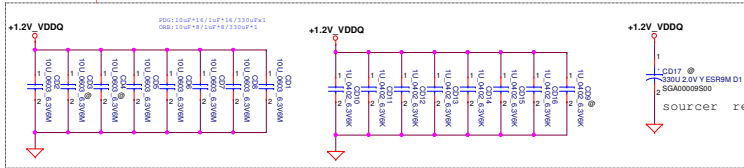
Non-ECC DIMM



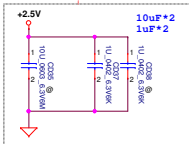
SPD ADDRESS FOR CHANNEL A :
 WRITE ADDRESS: 0XA0
 READ ADDRESS: 0XA1
 SA0 = 0; SA1 = 0; SA2 = 0.
 DDR4 POR OPERATING SPEED: 1867 MT/S
 STRETCH GOAL IS 2133 MT/S



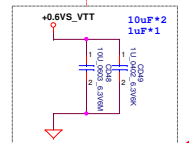
Layout Note:
Place near JDIMM1



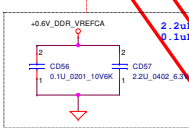
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1



Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE DIMM1



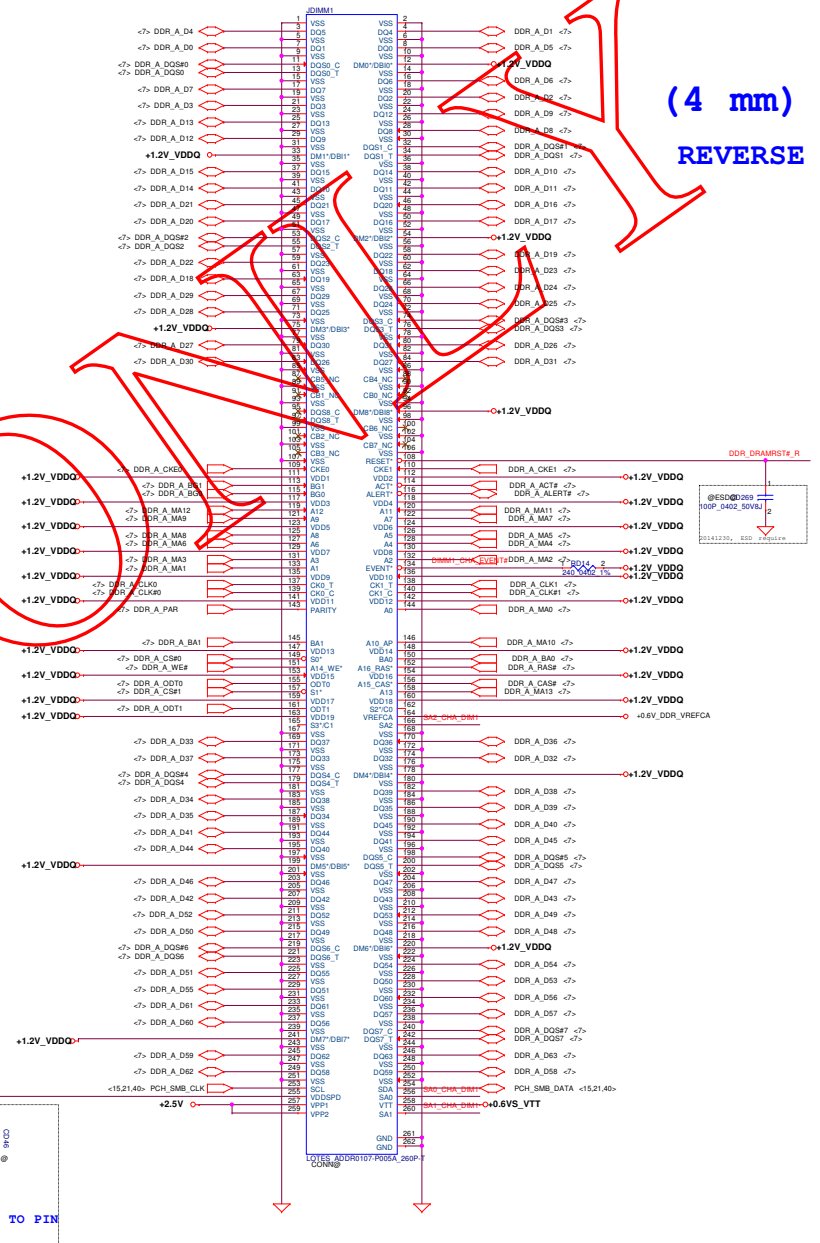
Place near SODIMM side,

DIMM1 Side

CPU Side

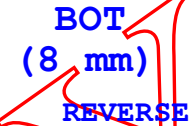
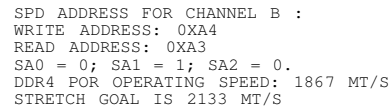
PLACE NEAR TO PIN

(4 mm)
REVERSE



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				Date	Friday, August 14, 2015
				Sheet	20 of 62

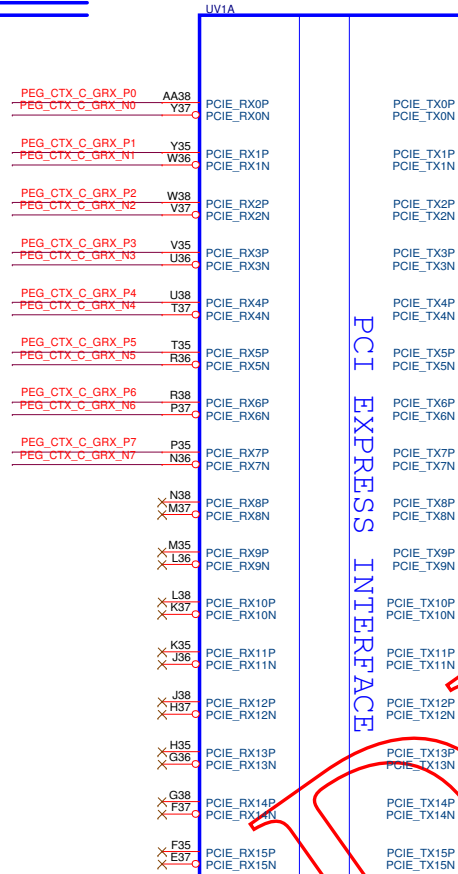
Non-ECC DIMM



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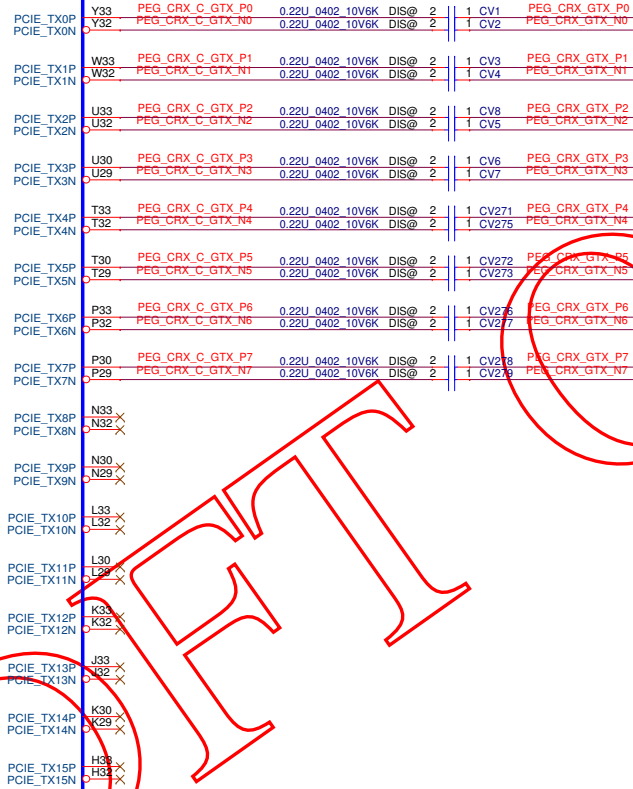
GFX PCIE LANE REVERSAL

<6> PEG_CTX_C_GRX_P[0..7]
<6> PEG_CTX_C_GRX_N[0..7]

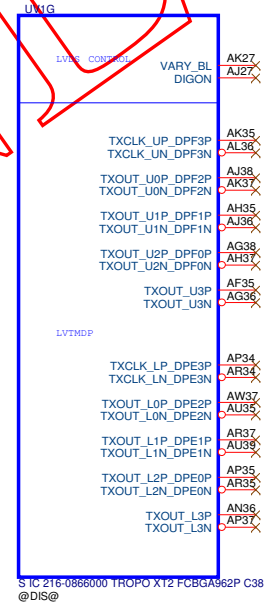


PCI EXPRESS INTERFACE

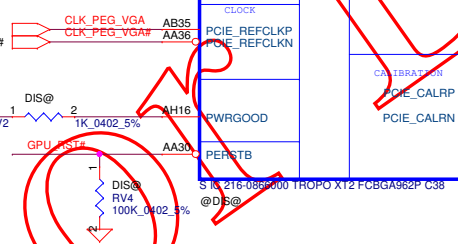
PEG_CRX_GTX_P[0..7]
PEG_CRX_GTX_N[0..7]



LVDS Interface

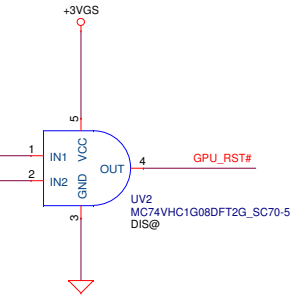


<16> CLK_PEG_VGA#
<16> CLK_PEG_VGA#



DIS@ RV1 1.69K_0402_1%
+VGA_PCIE
DIS@ RV3 1K_0402_1%
+VGA_PCIE

<17> DGPU_HOLD_RST#
<16,34,35,36,38,39,42> PLT_RST#



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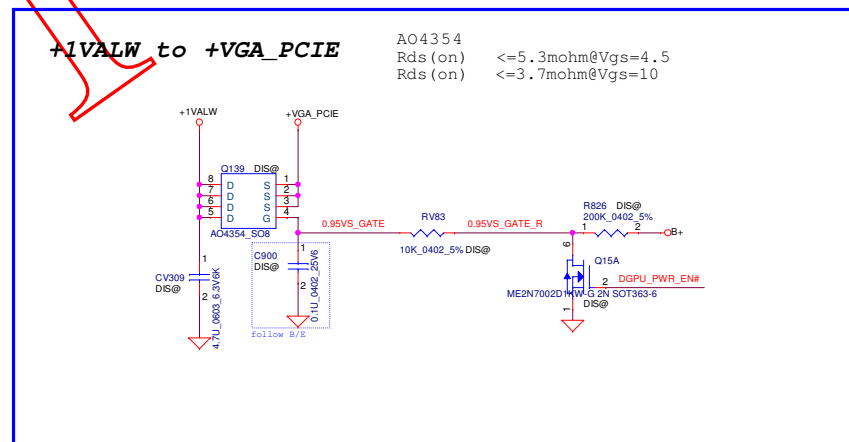
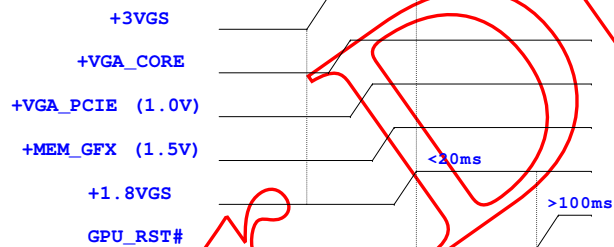
AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL
RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND
NOT CONFLICT DURING RESET

The image shows three circuit diagrams labeled PS1, PS2, and PS3. Each diagram represents a voltage divider circuit. A 1.8VGS voltage source is connected to a 10K resistor (RV03 for PS1, RV00 for PS2, RV01 for PS3). This resistor is in series with a 4.75K resistor (RV08 for PS1, RV09 for PS2, RV10 for PS3). The output of the divider is taken from the node between the two resistors and is connected to a 0.01uF capacitor to ground. The output voltage is labeled as 0.897V for PS1, 0.896V for PS2, and 0.896V for PS3. The resistors are labeled with their values and a 1% tolerance: 10K 0.02, 1% DIS and 4.75K 0.02, 1% DIS.

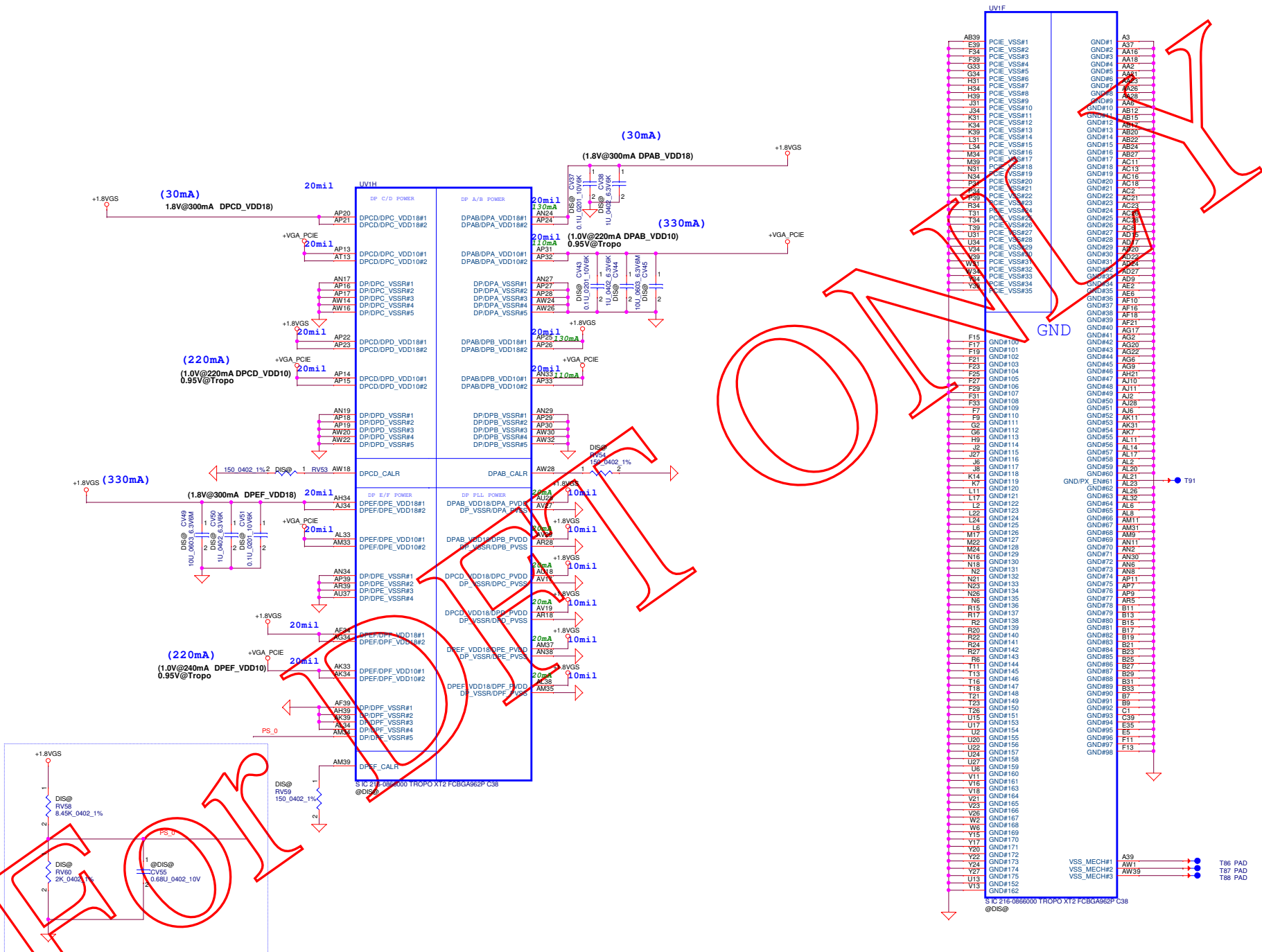
TROPO MLPs
PS 3 used default

```
PS3_[1] = 0 Reserved
PS3_[2] = 0 Reserved
PS3_[3] = 0 Reserved
PS3_[4] = 1 Audio-capable display outputs. 111 = No usable endpoints.
PS3_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.
```

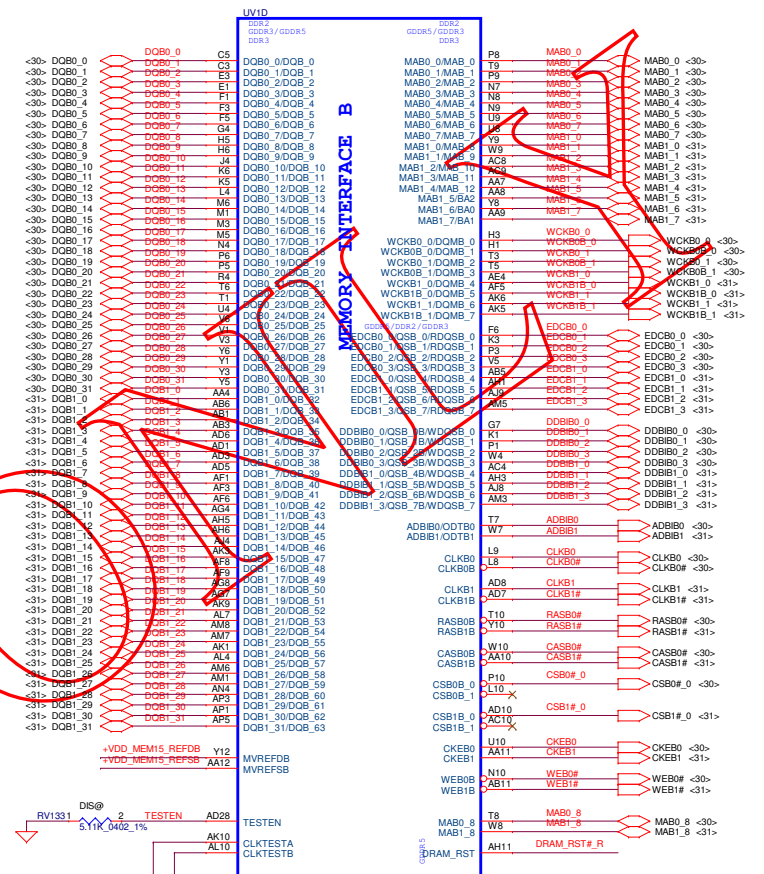
```
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF
```



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Issued Date		Deciphered Date		Title Tropo XT2(3/8) DC/DC POWER	
2015/08/10		2016/12/31		Size Document Number LA-C951P	
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Date:				Friday, August 14, 2015	
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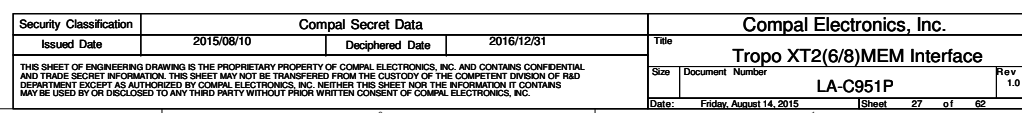
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/08/10	Deciphered Date	2016/12/31	Title	
				Tropo XT2(4/8)DPX Power/GND	
				Size	Rev
				Document Number	1.0
				Customer	LA-C951P
				Date	Friday, August 14, 2015
				Sheet	25 of 82



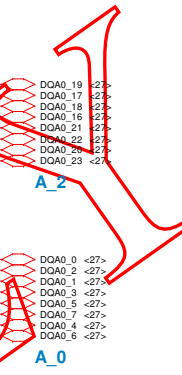
CV218 CV219
0.1U_0201_10V6K 0.1U_0201_10V6K

RV87 RV88
51.1_0402_1% 51.1_0402_1%

route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

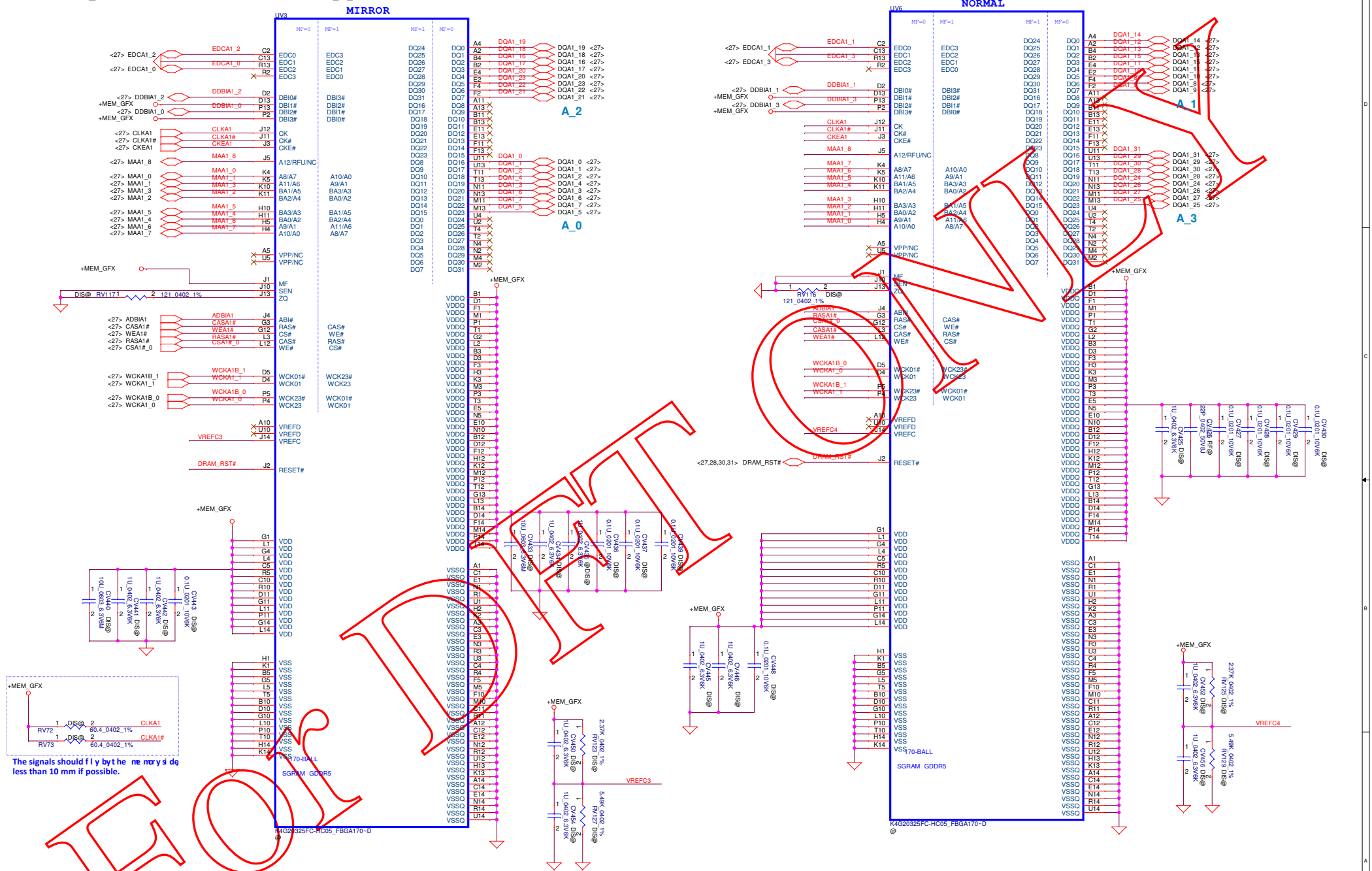


64X32 GDDR5



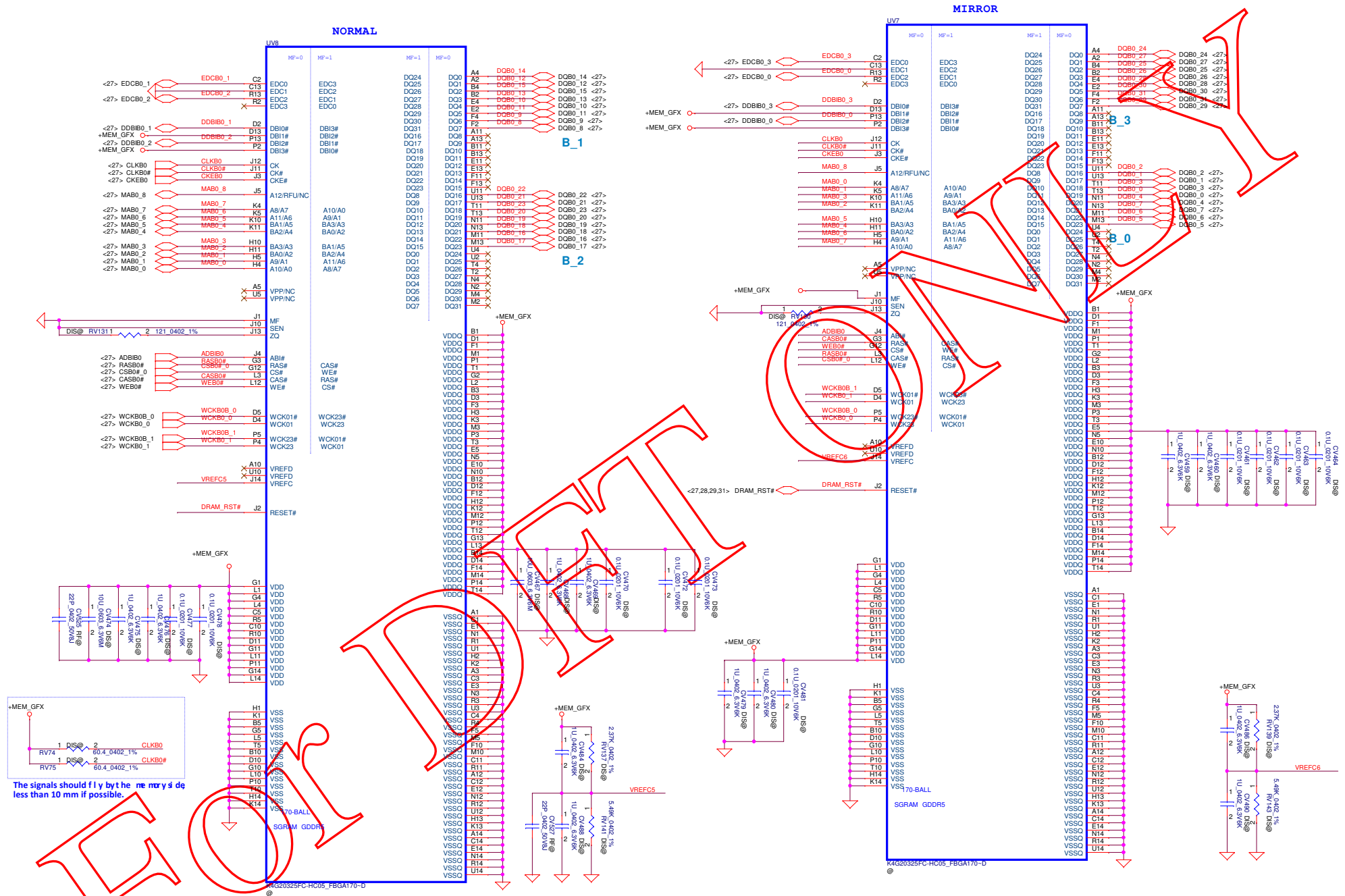
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Issued Date	2015/08/10	Deciphered Date	2016/12/31	Title VRAM A Lower UV14,UV15			
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Memory Partition A - Upper 16 bits

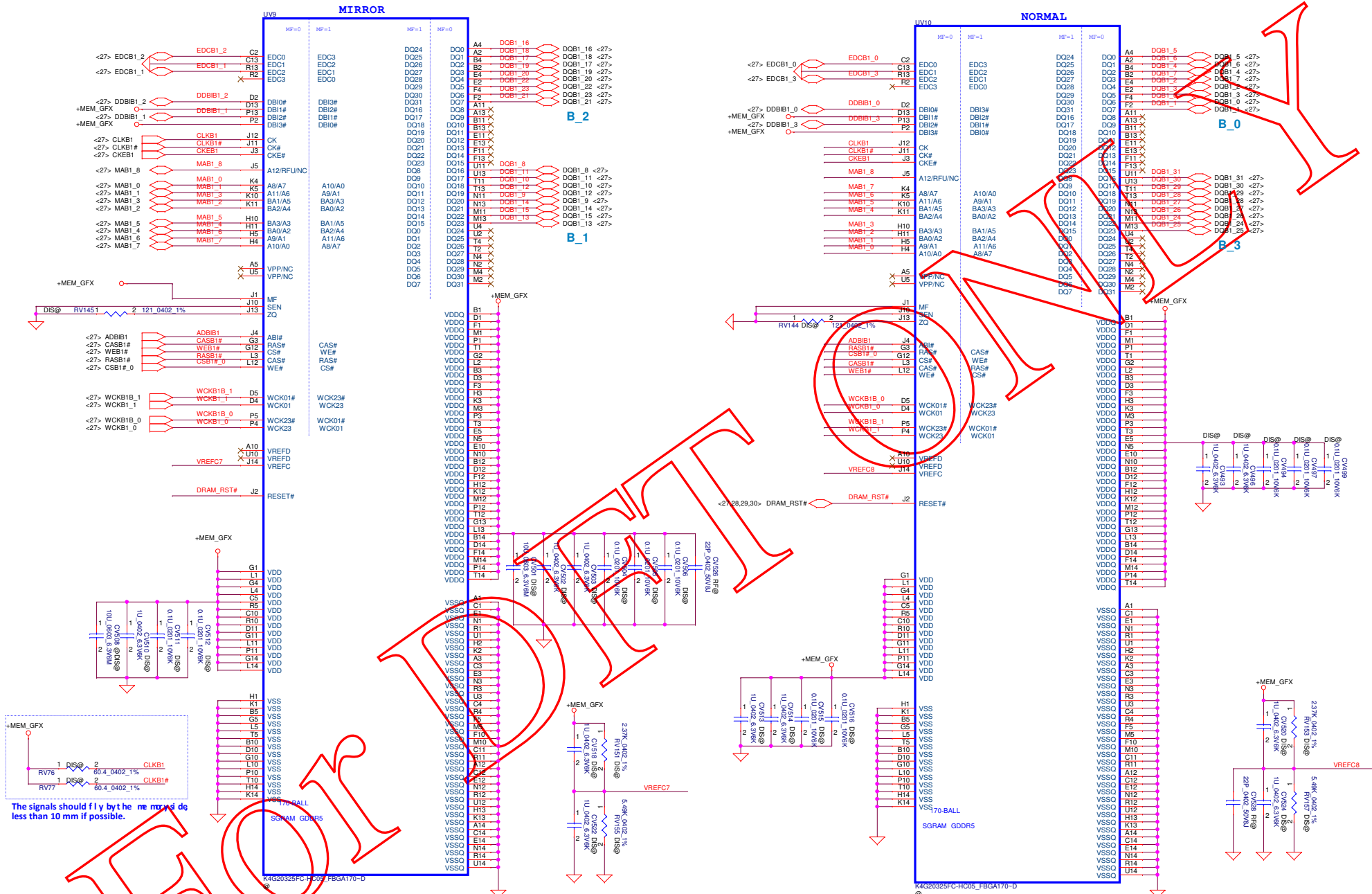


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Memory Partition B - Lower 16 bits



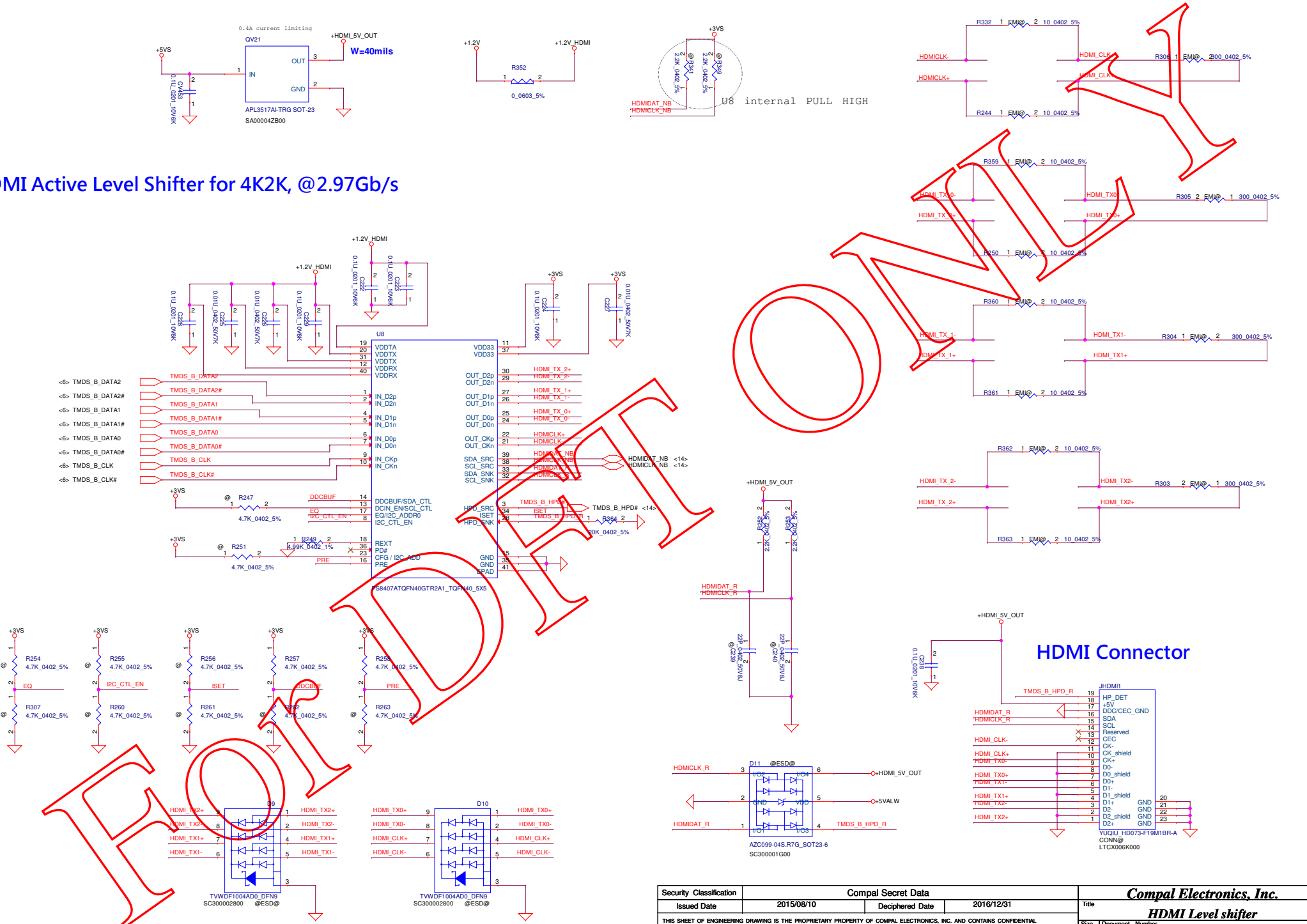
Memory Partition B - Upper 16 bits



The signals should fly by the net max delay less than 10 mm if possible.

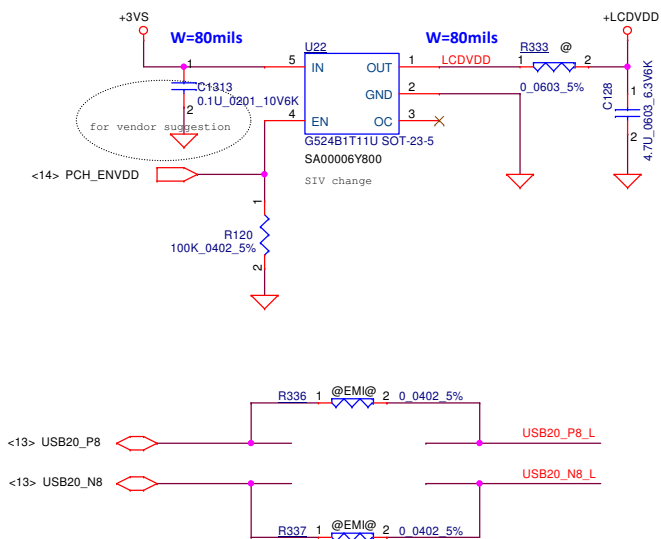
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								VRAM B Lower UV20,UV21	
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HDMI Active Level Shifter for 4K2K, @2.97Gb/s

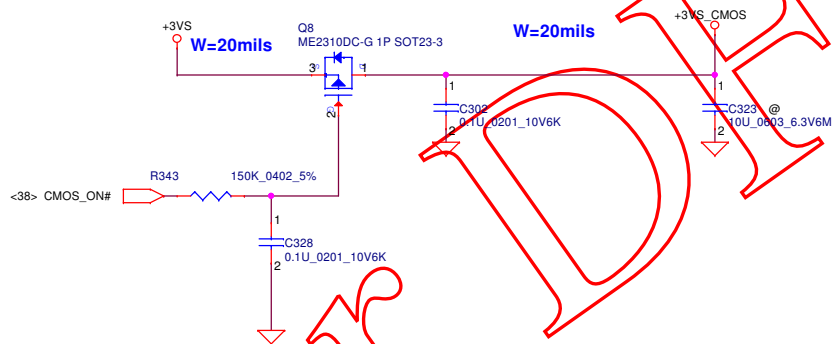


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				Size	Document Number	Rev
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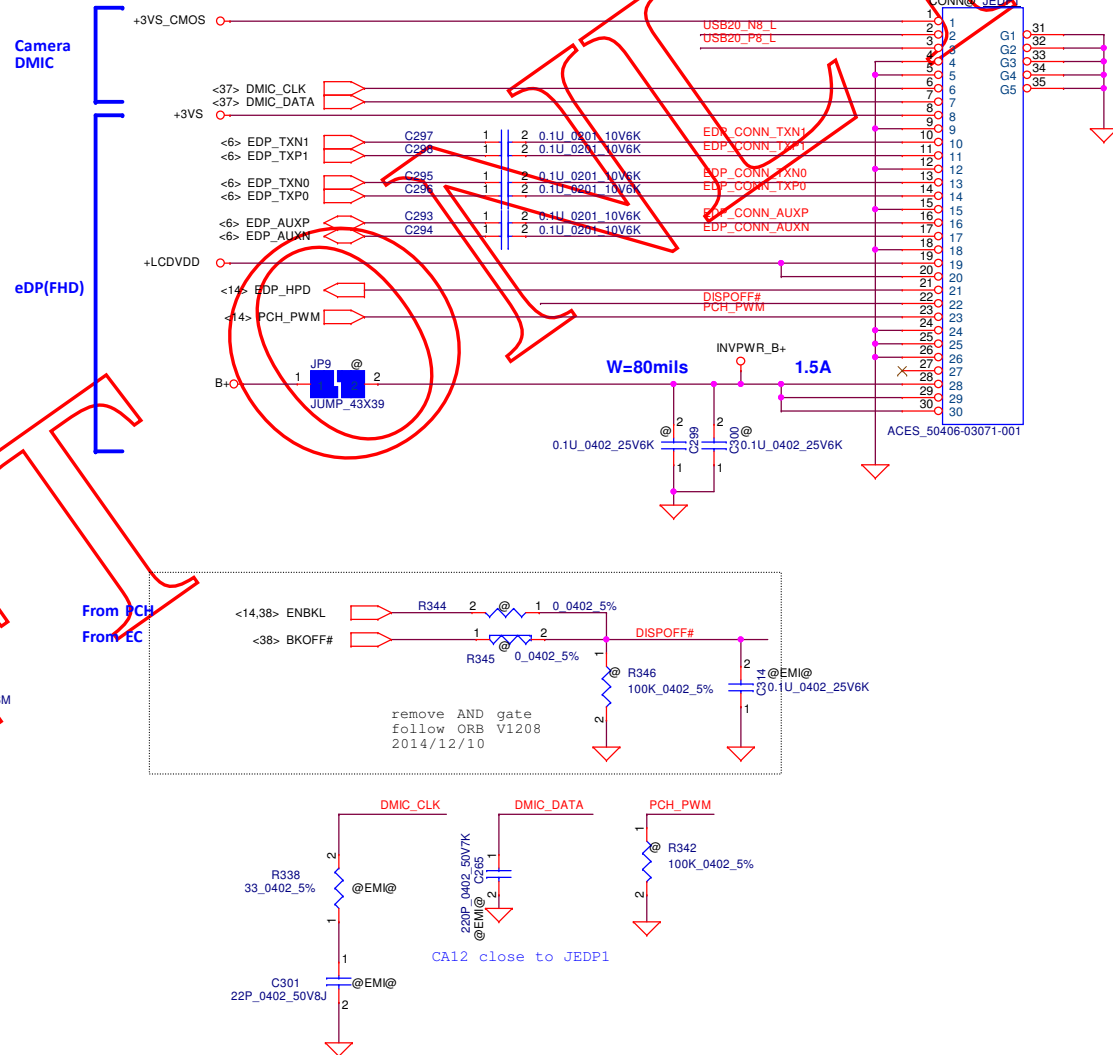
LCD POWER CIRCUIT



CMOS Camera



eDP(FHD) + Camera

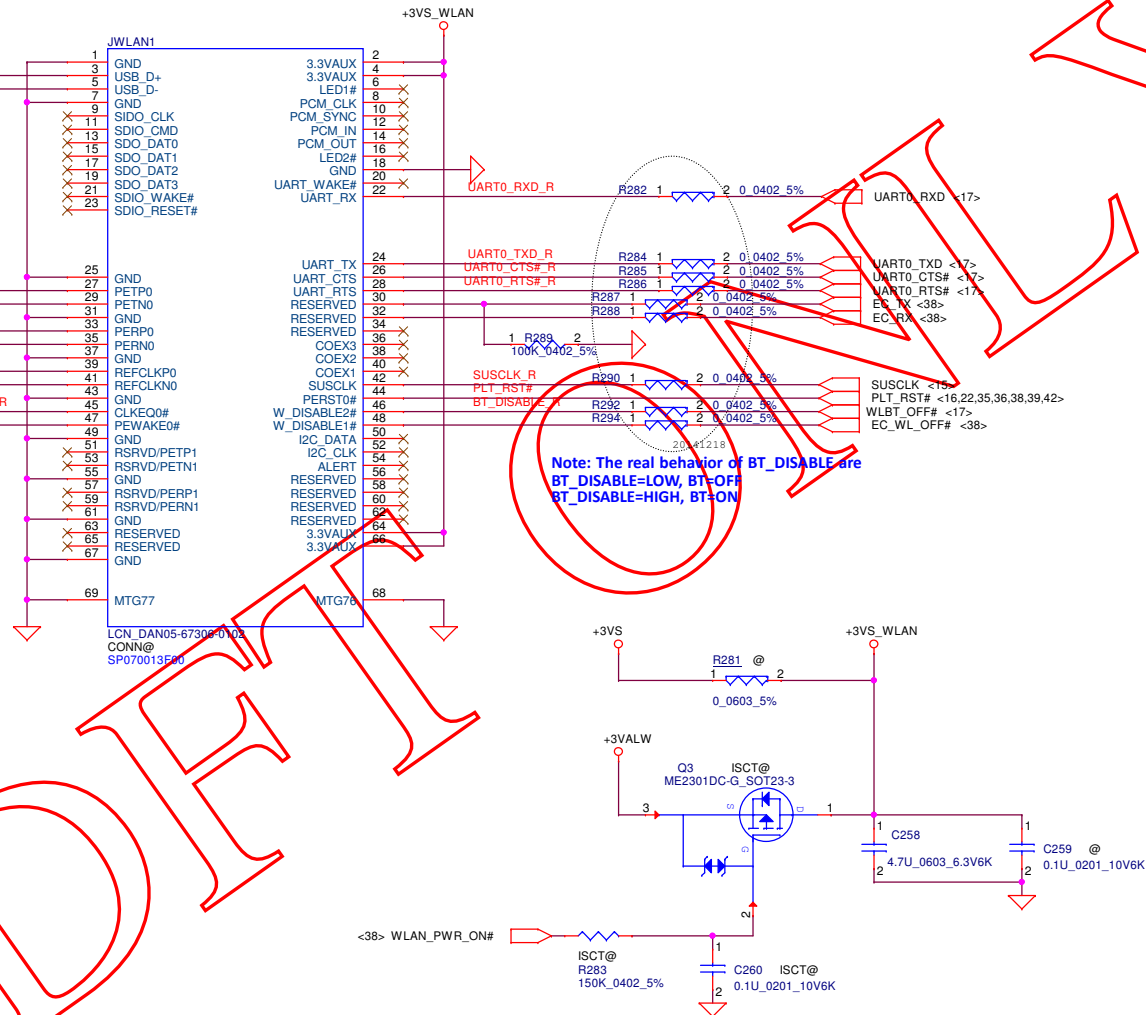


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NGFF for WLAN+BT E-KEY

BT

WLAN



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Size Custom	Document	Number	Rev	LA-C951P	
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Card Reader RTS5249S-QFN32

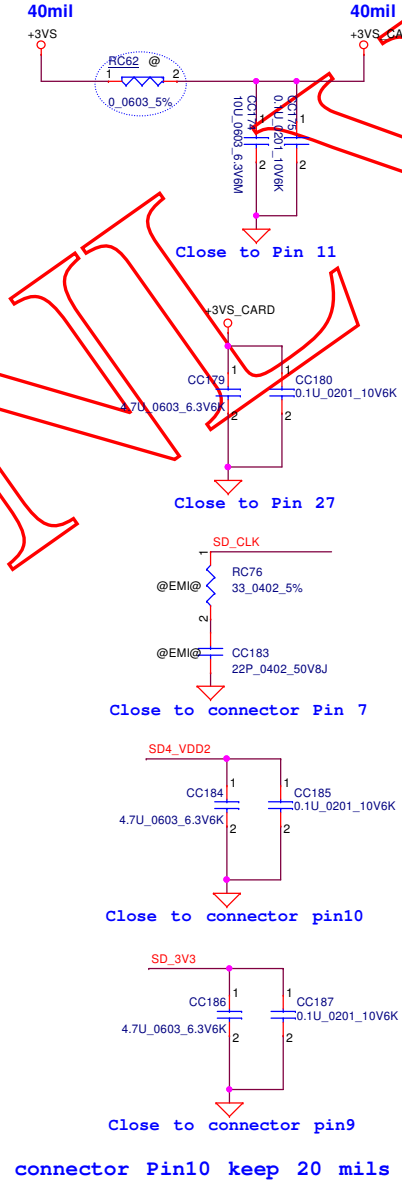
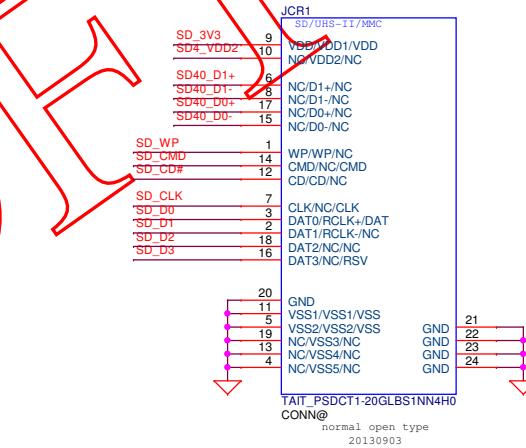
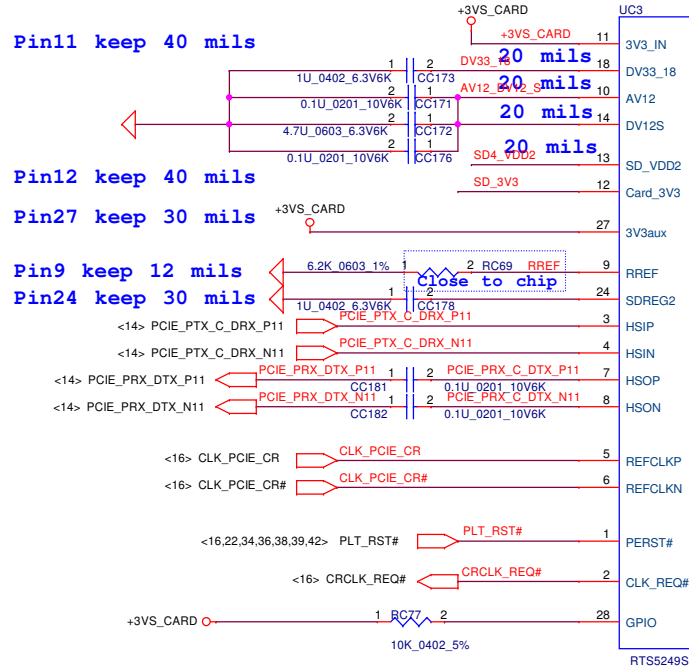
Pin11 keep 40 mils

Pin12 keep 40 mils

Pin27 keep 30 mils

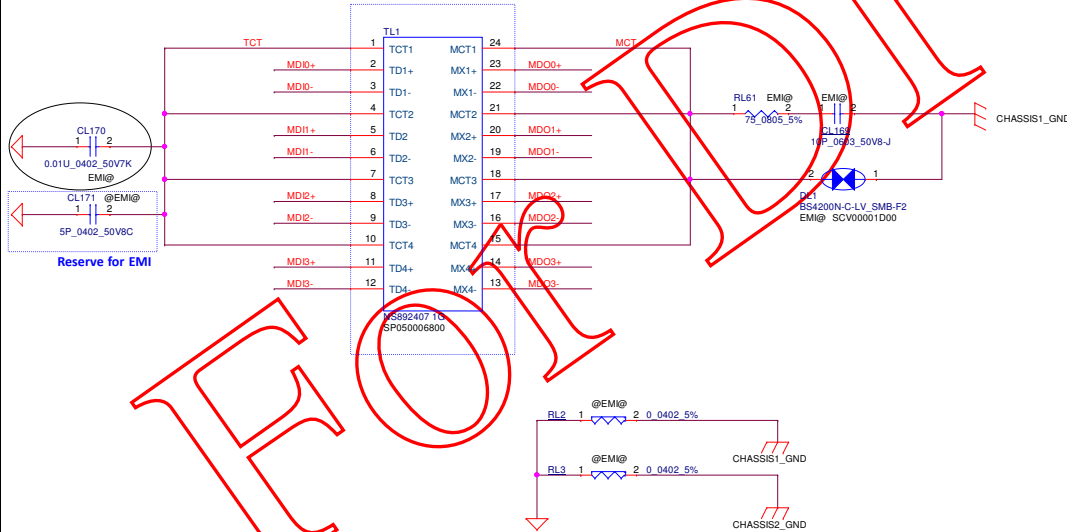
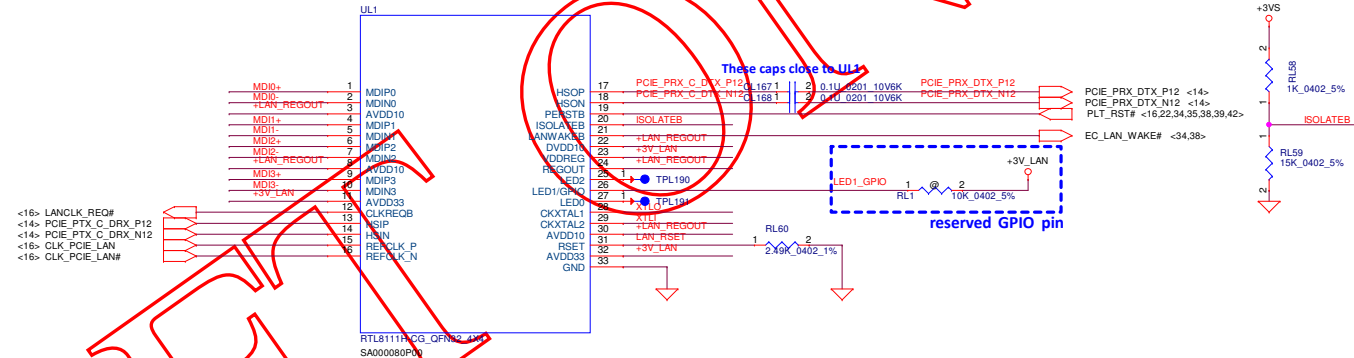
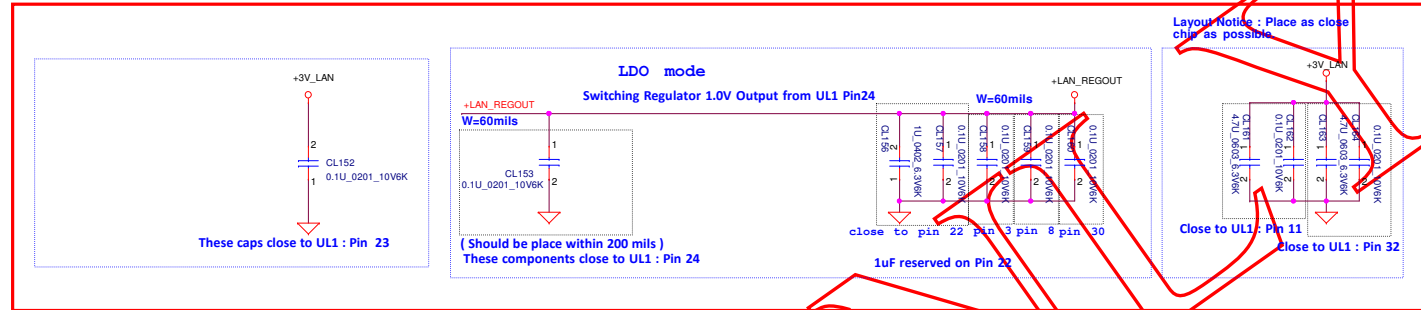
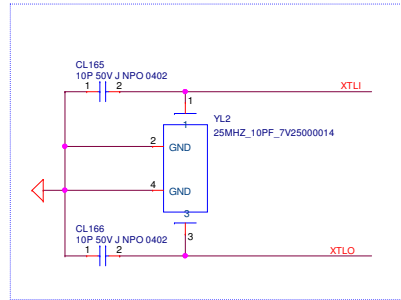
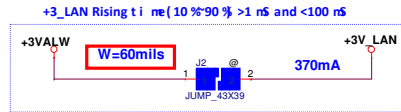
Pin9 keep 12 mils

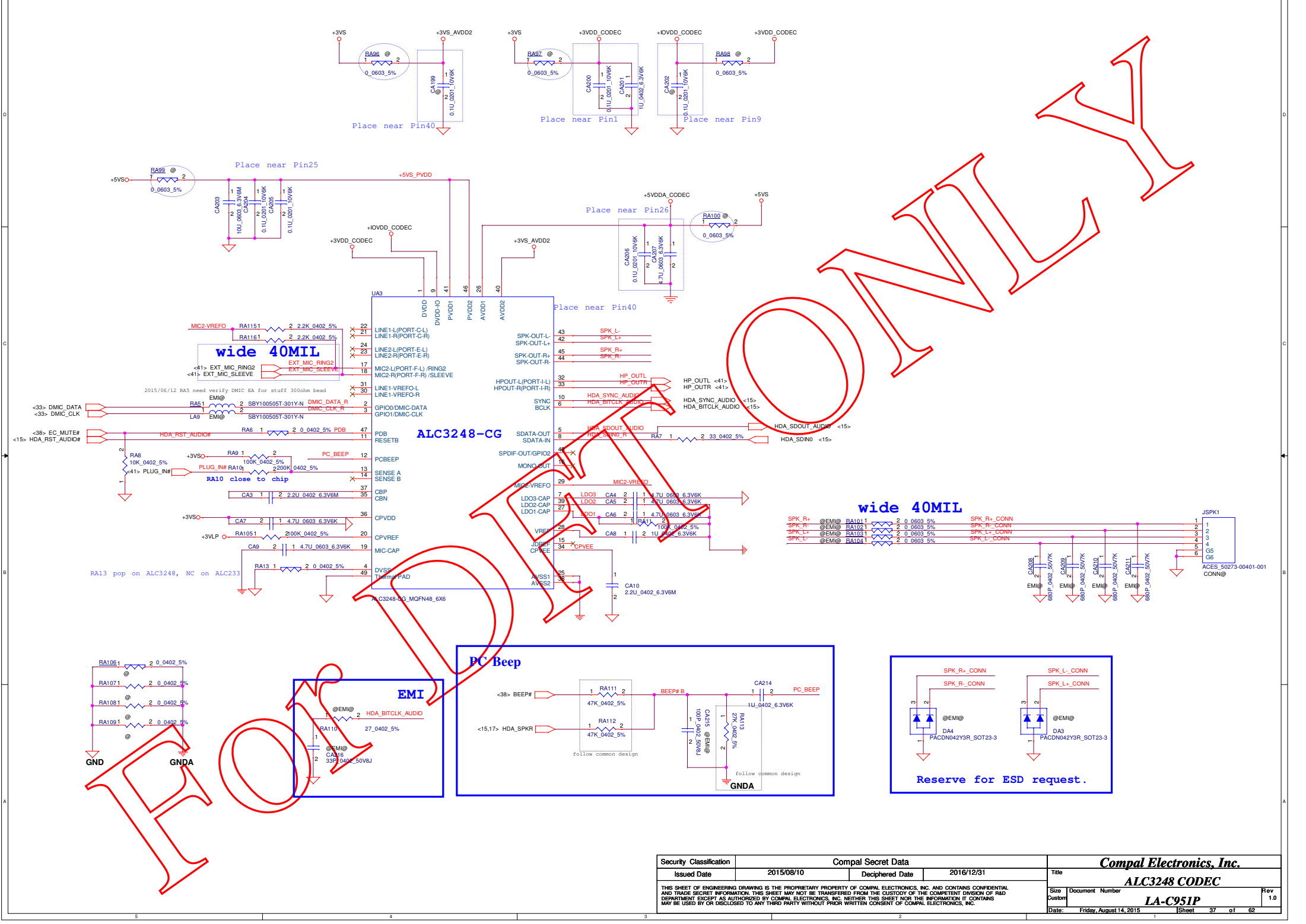
Pin24 keep 30 mils



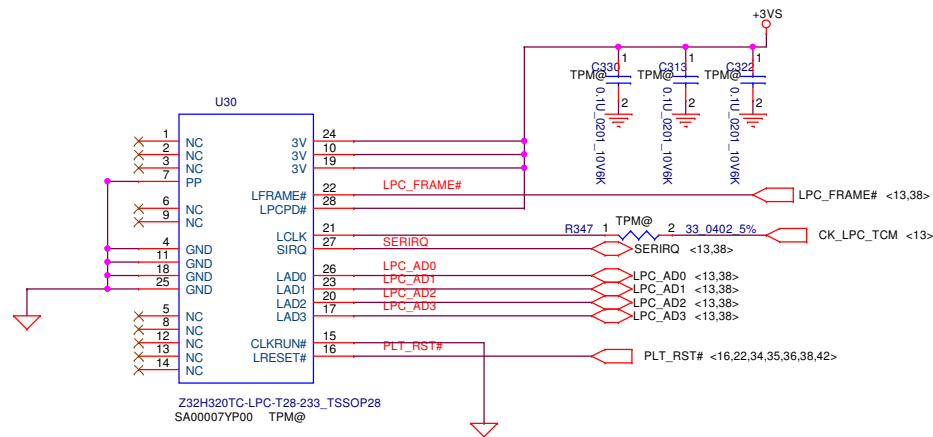
connector Pin10 keep 20 mils

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Custom		Document Number		1.0	
Date: Friday, August 14, 2015		Sheet		37 of 62	

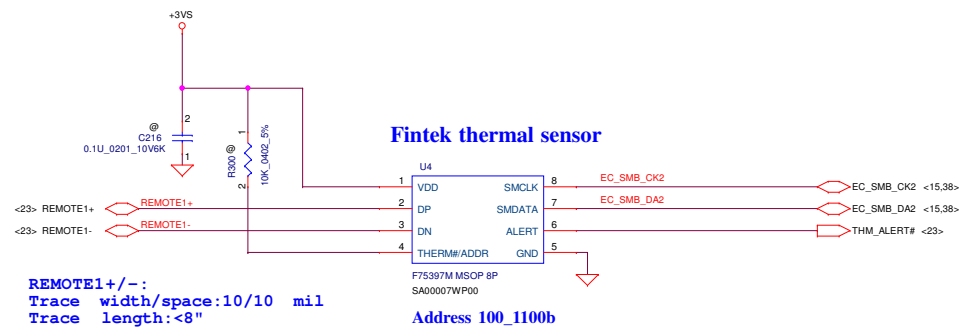


FOR DEF

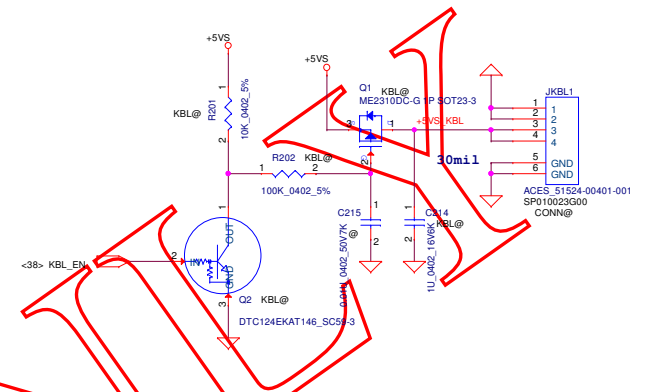
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				Size	Document Number	Rev
				Custom	LA-C951P	1.0
Date:		Friday, August 14, 2015		Sheet	39 of 62	

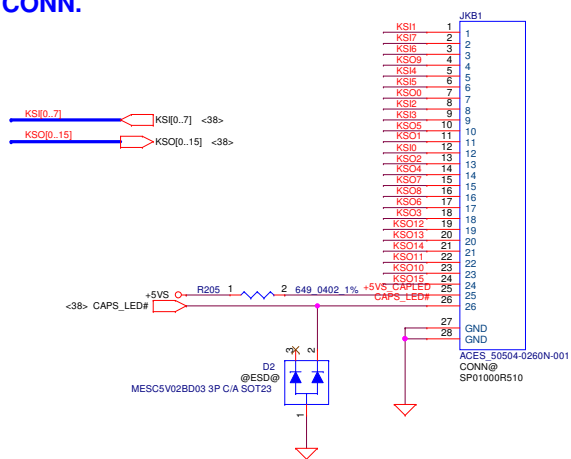
Thermal Sensor



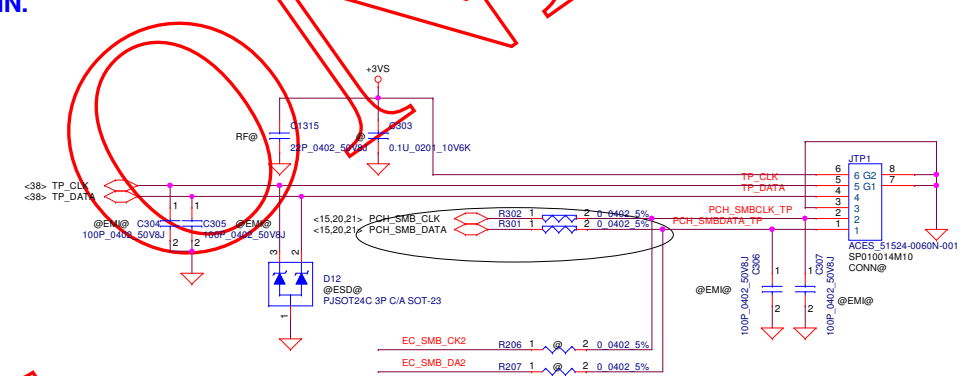
KB BKL



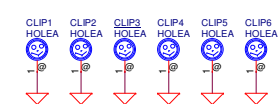
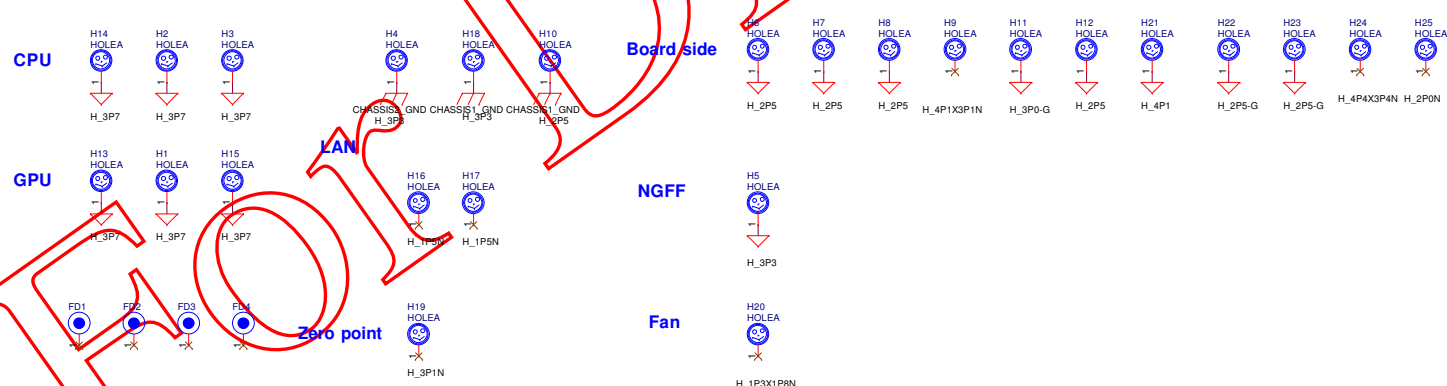
KB CONN.



TP CONN.

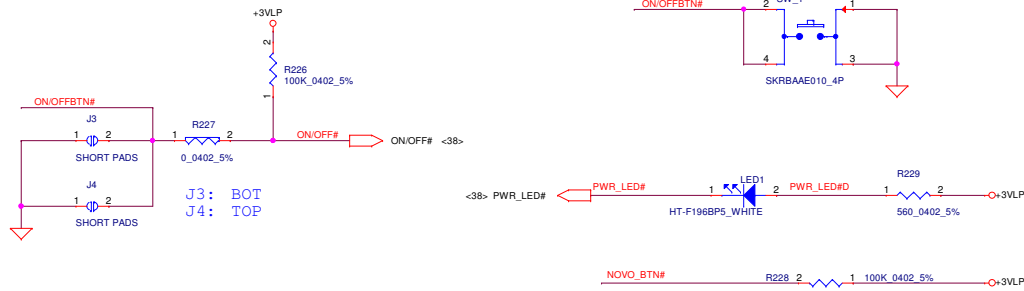


Screw

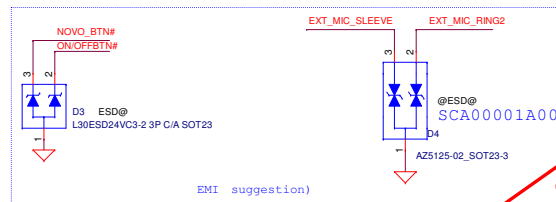
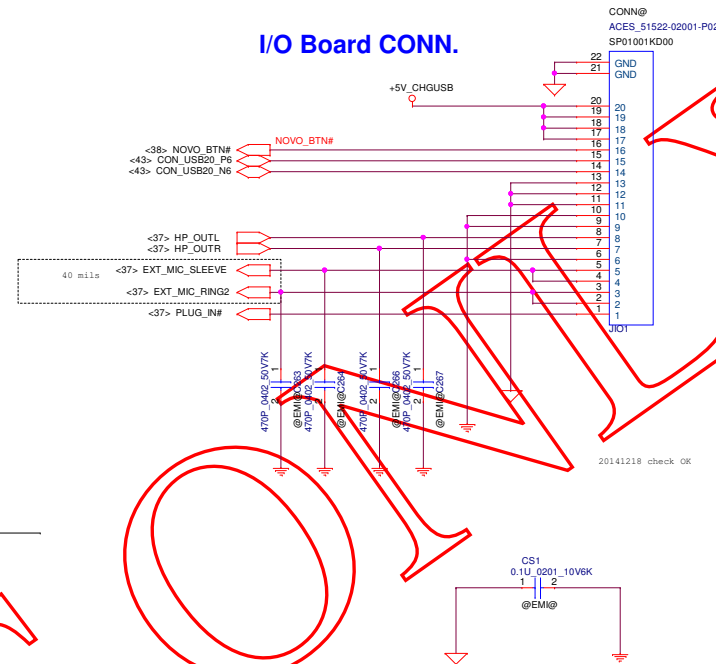


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Issued Date	2015/08/10	Deciphered Date	2016/12/31	Title	KB/TP/Thermal Sensor	
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				Document Number		
				Date:	Friday, August 14, 2015	Sheet 40 of 62

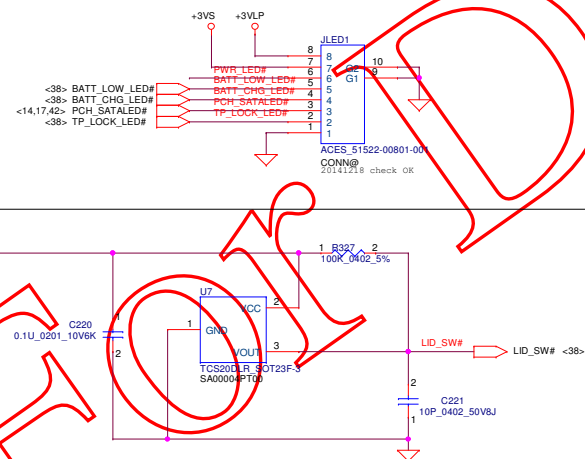
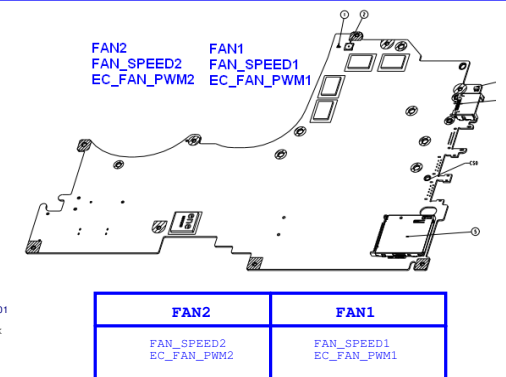
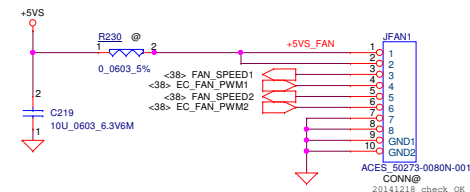
Power BTN.

Power_BTN

I/O Board CONN.

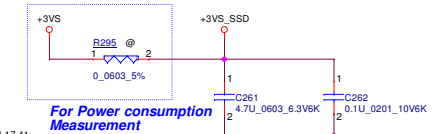
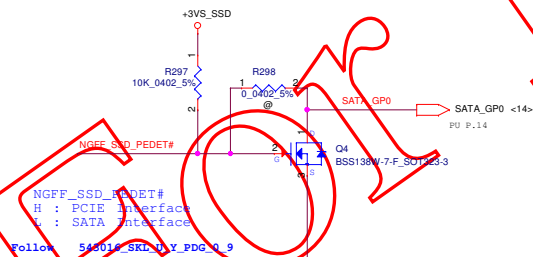


LED Board CONN.

**FAN1 Conn**

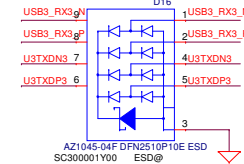
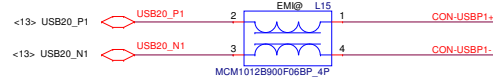
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Date: Friday, August 14, 2015				Sheet	41 of 62

**SATA SSD CONN.
M-KEY**



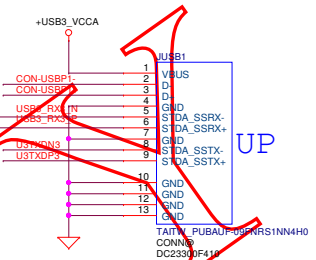
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Issued Date	2015/08/10	Deciphered Date	2016/12/31	Title	
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				Sheet	LA-C951P
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USB3.0 <Port1,Port2>

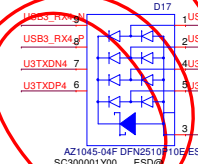
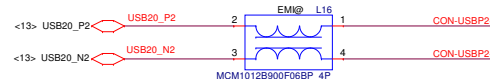
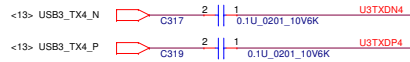


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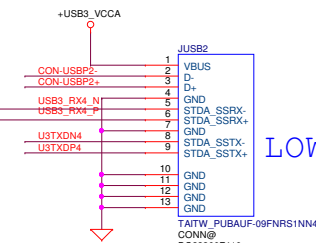


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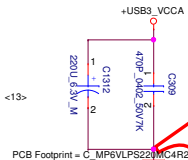
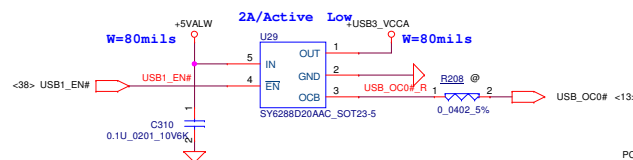


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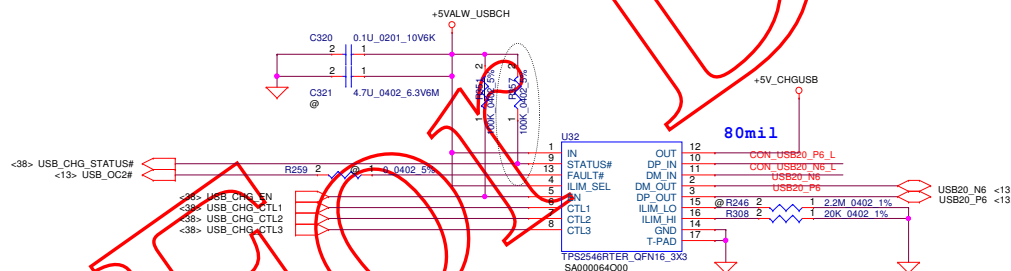


LOW

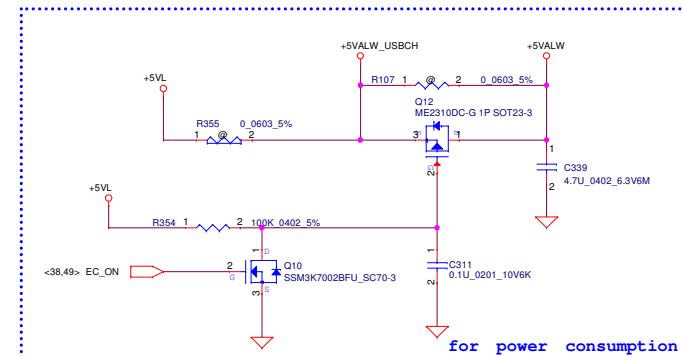
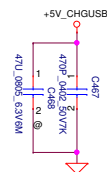
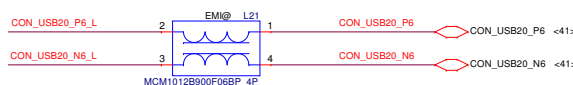


PCB Footprint = C_MP6VLP5220MC4R2

USB2.0 + Charger



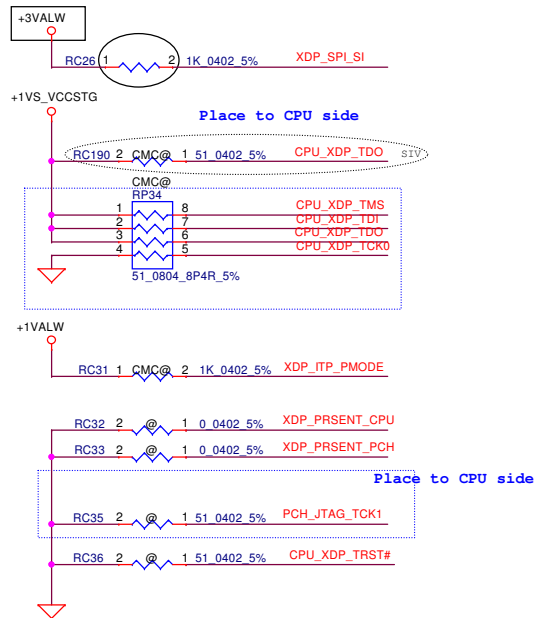
	CTL1	CTL2	CTL3
S0	H	H	H
S3	H	H	H
DC S5	L	L	H



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								Rev			
								1.0			
								LA-C951P			
								Date: Friday, August 14, 2015			
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PRIMARY CMC TP



<11,15> CPU_XDP_TDO CPU_XDP_TDO TP@ TC245
 <11,15> CPU_XDP_TDI CPU_XDP_TDI TP@ TC246
 <11,15> CPU_XDP_TMS CPU_XDP_TMS TP@ TC247
 <11,15> CPU_XDP_TCK0 CPU_XDP_TCK0 TP@ TC249
 <11,19> CPU_XDP_TRST# CPU_XDP_TRST# TP@ TC248
 <15> PCH_JTAG_TCK1 PCH_JTAG_TCK1 TP@ TC250

<16> XDP_SPI_SI XDP_SPI_SI TP@ TC251
 <15> XDP_ITP_PMODE XDP_ITP_PMODE TP@ TC252

<11,19> XDP_PREQ# XDP_PREQ# TP@ TC253
 <11,19> XDP_PRDY# XDP_PRDY# TP@ TC254

<11> CFG0 CFG0 TP@ TC225
 <11> CFG1 CFG1 TP@ TC226
 <11> CFG2 CFG2 TP@ TC227
 <11> CFG3 CFG3 TP@ TC228
 <11> CFG4 CFG4 TP@ TC229
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 <11> CFG6 CFG6 TP@ TC231
 <11> CFG7 CFG7 TP@ TC232

<11> CFG17 CFG17 TP@ TC233
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<11> CFG8 CFG8 TP@ TC235
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 <11> CFG15 CFG15 TP@ TC242

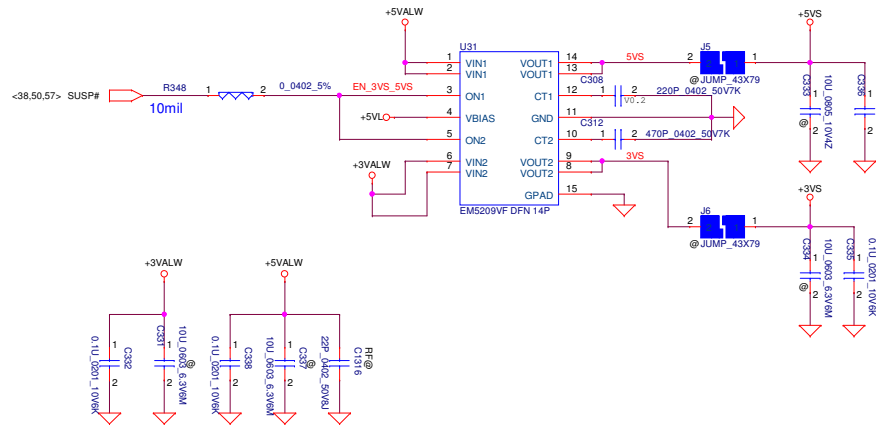
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 <11> CFG18 CFG18 TP@ TC244

<16> XDP_SPI_IO2 XDP_SPI_IO2 TP@ TC255
 <16> XDP_SPI_IO2 XDP_SPI_IO2 TP@ TC256

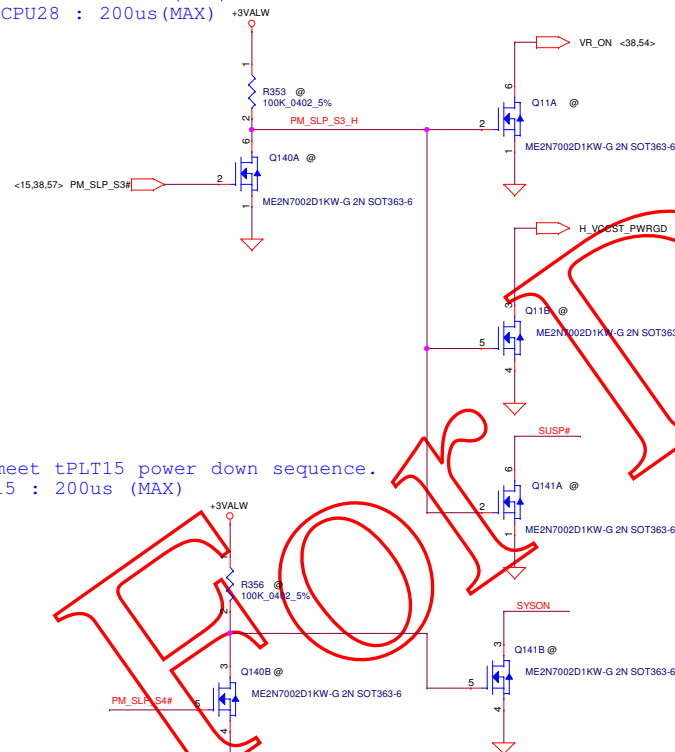
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										CMC debug port	
										LA-C951P	
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										Date: Friday, August 14, 2015	
										Sheet 44 of 62	

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+5VALW TO +5VS
+3VALW TO +3VS



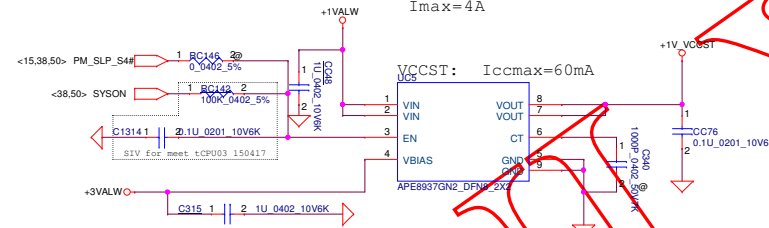
For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 200us (MAX)
tPLT18 : 200us (MAX)
tCPU28 : 200us (MAX)



For meet tPLT15 power down sequence.
tPLT15 : 200us (MAX)

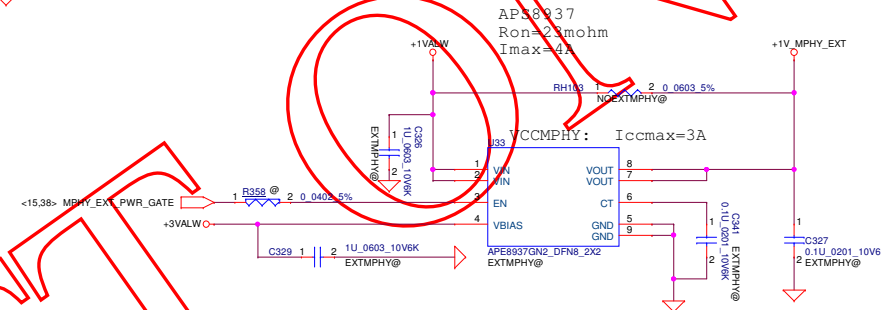
+1VALW TO +VCCST

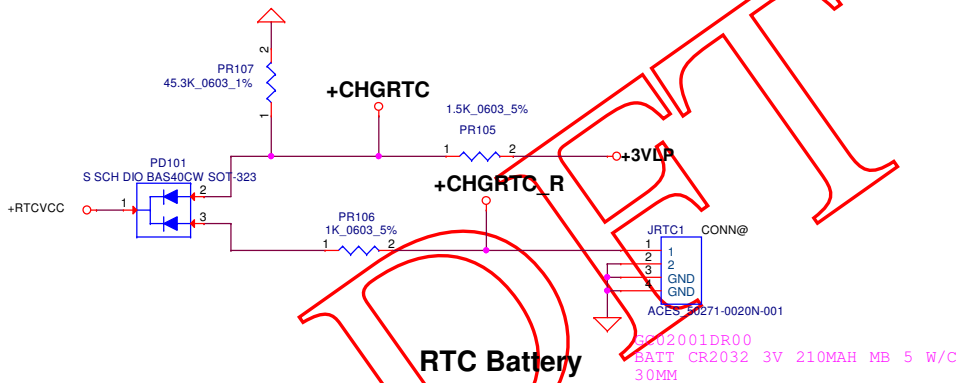
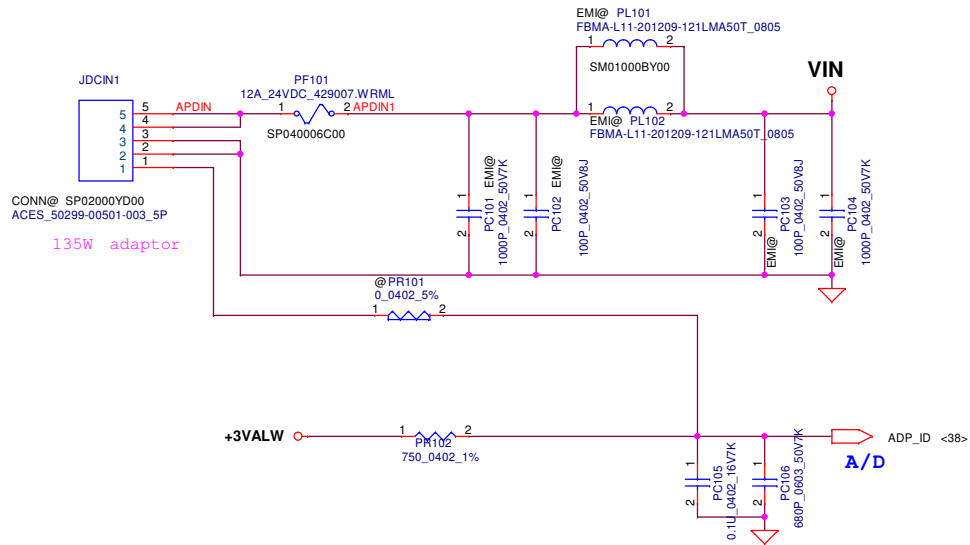
APS8937
Ron=23mohm
Imax=4A



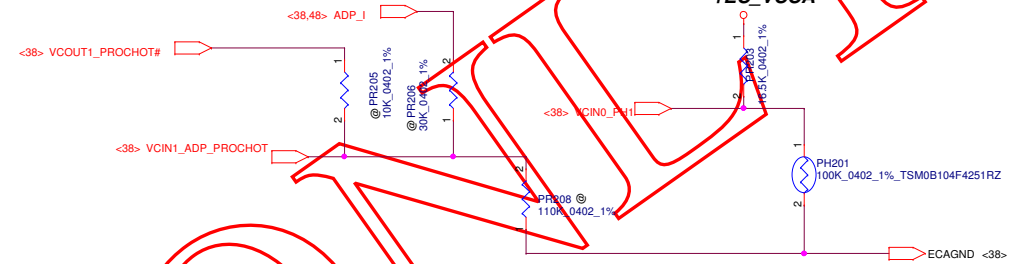
+1VALW TO +VCCMPHY

APS8937
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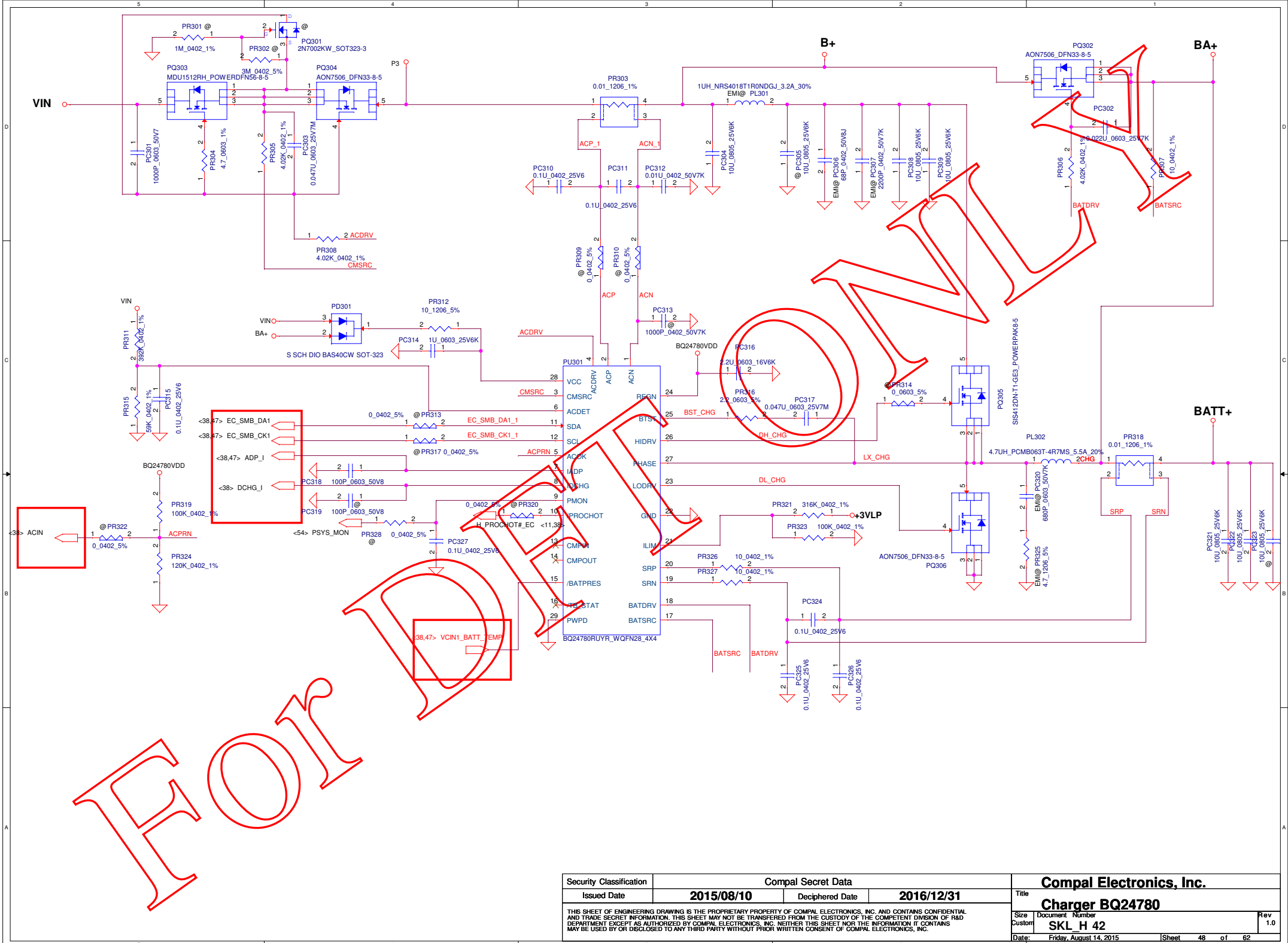




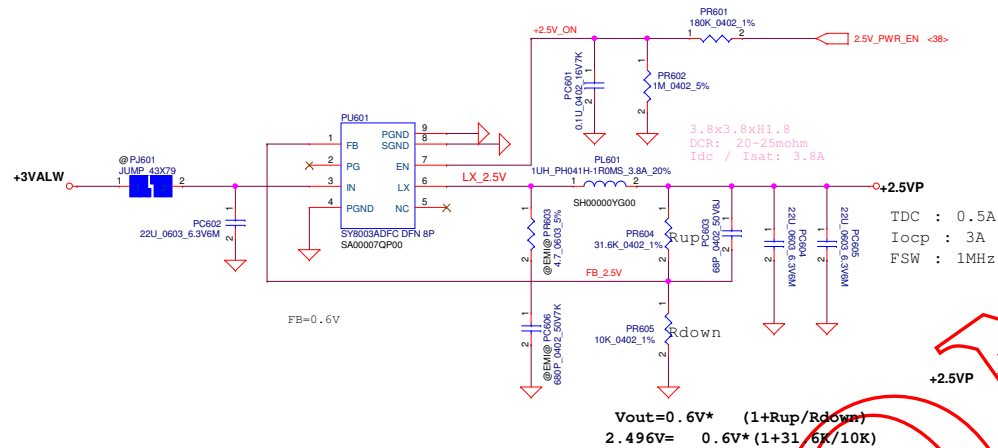
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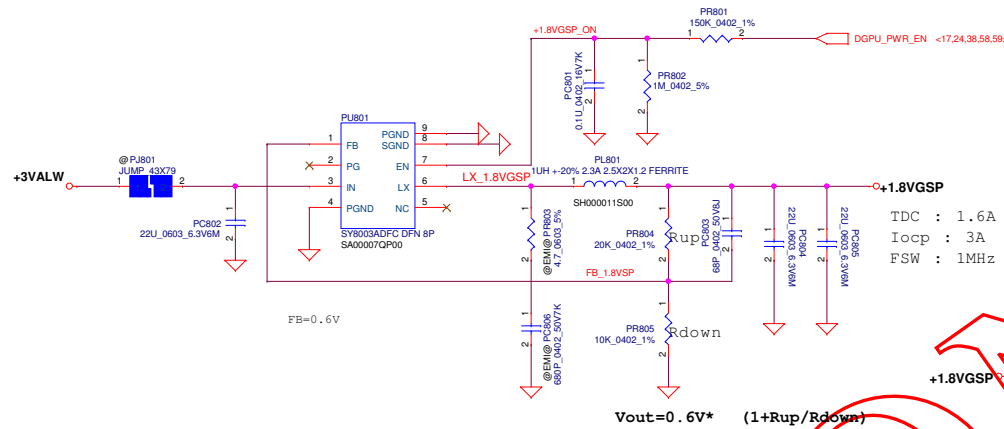
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Issued Date	2015/08/10	Deciphered Date	2016/12/31	Title	PWR-BATTERY CONN/OTP	
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Size	Custom	Document Number	SKL H 42	Rev 1.0
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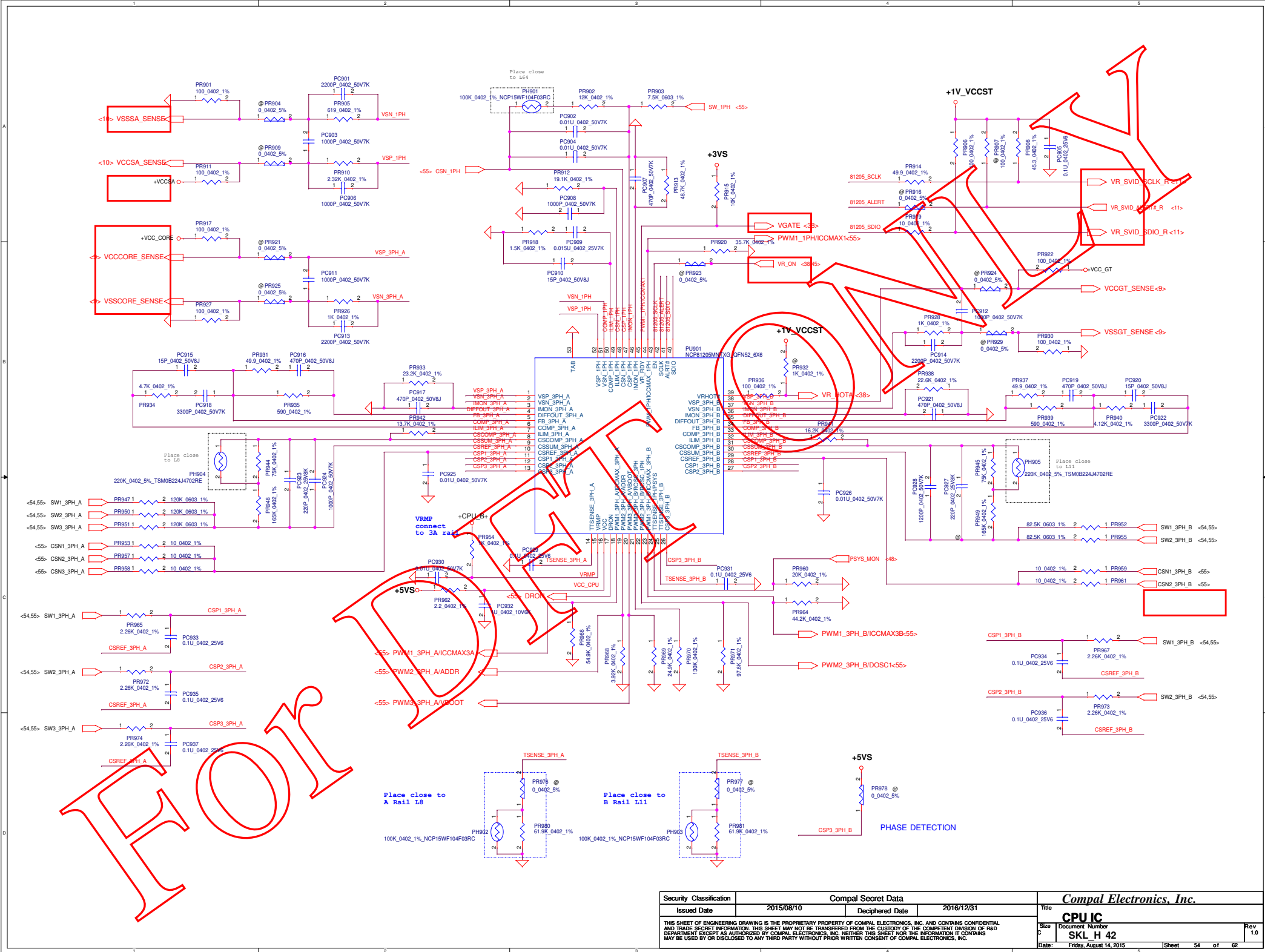


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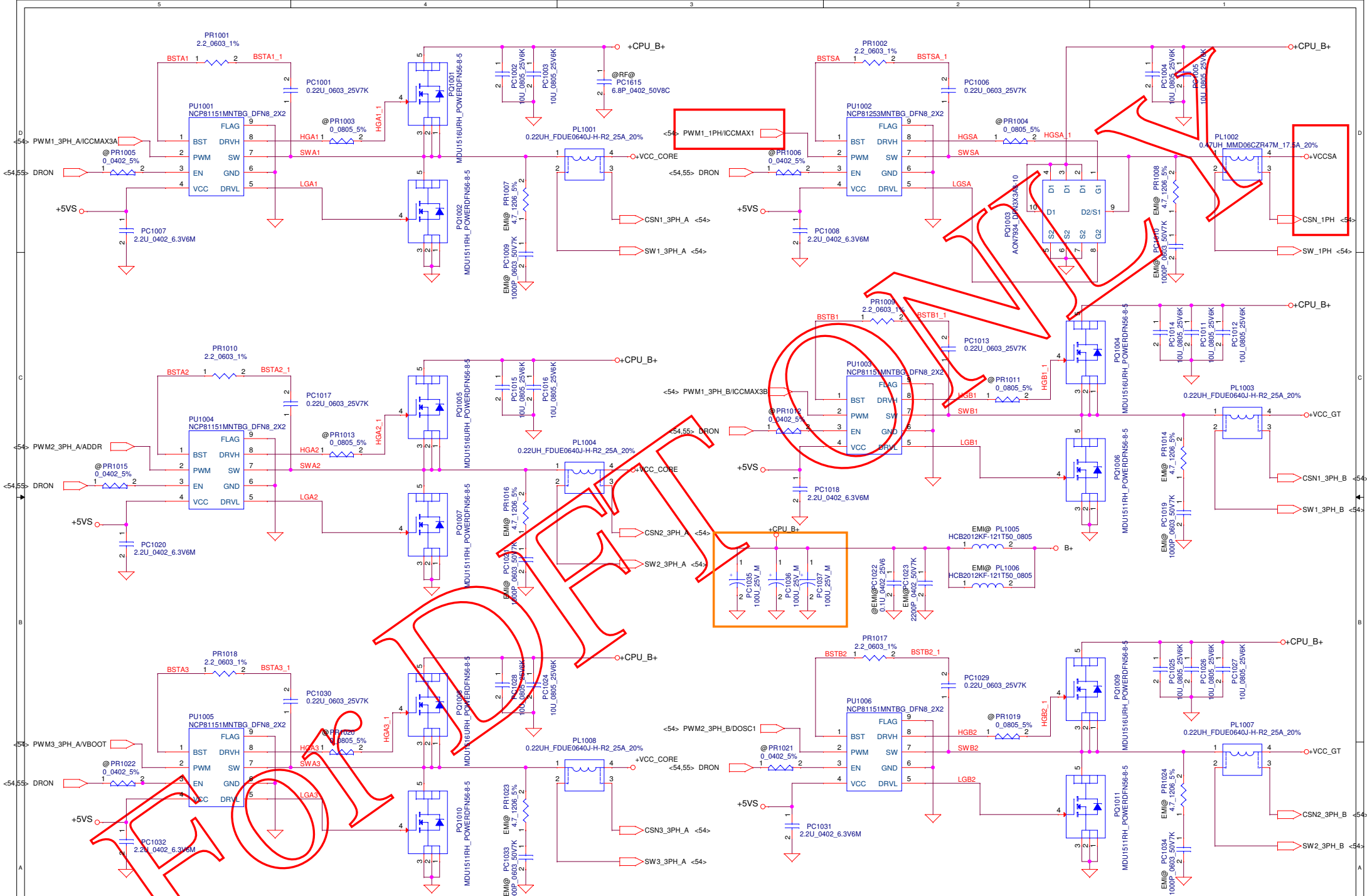


+1.8VGSP
 JUMP_43X79
 +1.8VGS

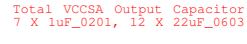
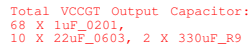
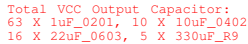
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Sheet		Document Number		Rev	
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Compal Electronics, Inc.

Processor decoupling

Document Number
SKL_H 42

1.0

Version change list (P.I.R. List)

Page 1 of 2
for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW design	41	Add DGPU_PWR_EN to EC pin71 Reserve LAN_WAKE# test point at EC pin66 Add R830 PU 10k to 3VALW for EC_LAN_WAKE#	04/07	SIV
2	HW design	9	add TC255~260 on UC1.B2, UC1.B38, UC1.BP1, UC1.BR2, UC1.C1, UC1.C38 TestPoint for SMT test	04/08	SIV
3	HW design	18	remove RH73, CH30 for DCPDSW_1P0 is output pin	04/08	SIV
4	HW design	36	add RC190 for CPU_XDP_TDO PULL high	04/08	SIV
5	HW design	17	RH105 stuff for KB_RST# is OD	04/08	SIV
6	HW design	42	JEDP1 conn. Pin define update	04/08	SIV
7	HW design	35	R228 stuff for novo_btn#	04/08	SIV
8	HW design	16	Change ch19, ch20 to 8.2p for meet X'tal spec	04/09	SIV
9	HW design	31	Change CL165, CL166 to 10p	04/09	SIV
10	HW design	42	C289,R334,C292,R335,C290,C291,U22 circuit change to R120,U5,C128,C1313	04/09	SIV
11	HW design	18	RH66,RH67,RH71,RH72,RH75,RH76,RH78 ,RH79,RH80,RH81,RH82,RH83,RH84 change to short pad	04/10	SIV
12	HW design	32	RC62 change to short pad	04/10	SIV
13	HW design	34	RA96,RA97,RA99,RA100 change to short pad	04/10	SIV
14	HW design	42	R336,R337,R338 change to short pad	04/10	SIV
15	HW design	8	RC83 change to short pad	04/10	SIV
16	HW design	11	RD3,RD5 change to short pad	04/10	SIV
17	HW design	38	R280 change to short pad	04/10	SIV
18	HW design	39	R281,R295 change to short pad	04/10	SIV
19	HW design	35	R230 change to short pad	04/10	SIV
20	HW design	33	R235~R242 change to short pad	04/10	SIV
21	HW design		RC43,RC49,RC54,RC57,RC81,RC83,RC189,RD4,RD8,RD12,RD22 ,RD26,RD28,RD36,RH51,R208,R323,R324,R314,R322,R331 ,RH40,RH42,RH43,RH46,R350,RA98 change to short pad	04/10	SIV
22	RF recommend	13	Add CH277,CH278 (@RF@)	04/16	SIV
23	HW design	40	RC142 change to 100kohm, add C1314(0.1u) for meet tCPU03	04/17	SIV
24	HW design	9	Delete TC257	04/20	SIV
25	HW design	10	Add TC263,TC264	04/20	SIV
26	RF recommend	11	Add CD271, CD272 for RF request	04/20	SIV
27	HW design	35	Update I/O board pindefine	04/21	SIV
28	EC recommend	15	Add RH108 reserve AC_PRESENT between EC and PCH	04/24	SIV
29	HW design	18	Add RH106(@),RH107	04/24	SIV

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Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
30	HW design	38	EC pin1 EC_LAN_WAKE# chagne to pin19, pin19 MPHY_EXT_PWR_GATE change to pin38 delete pin64 VCIN1_BATT_DROP, DCHG_I change from pin76 to 64pin	06/01	SIT
31	HW design	18	add RH118 between +3V_PCH and +3V_HDA for intel sighting 16 change RH80 from short pad to 0ohm and add CH279 for +1V_HDAPLL for intel sighting 16	06/01	SIT
32	HW design	32	R249 change to 4.99k, R263 change to non-stuff for HDMI EA R332,R244,R359,R250,R360,R361,R362,R363 change from 8.2ohm to 10ohm, R303,R304,R305,R306 change from 150ohm to 300ohm for HDMI EA	06/05	SIT
33	EMI design	37	CA208, CA209, CA210, CA211 change to 680p and stuff for EMI request	06/08	SIT
34	RF design	40	add C1315 for RF request	06/09	SIT
35	RF design	45	Jadd C1316 for RF request	06/09	SIT
36	RF design	30	add CV525,CV527, for RF request	06/10	SIT
37	RF design	28	CV392 change to 22p for RF request	06/10	SIT
38	RF design	29	CV426 change to 22p for RF request	06/10	SIT
39	RF design	31	add CV526, CV528 for RF request	06/10	SIT
40	EMI design	37	RA5 change to 300ohm bead for EMI request	06/22	SIT
41	HW design	6	PEG change to Lanes 8:15 / DEVICE0 (544924_544924_SkyLake_EDS_Vol_1_Rev_0.99)	06/22	SIT
42	ESD design	41	D3 change to SCA00001G00 for ESD request	06/22	SIT
43	ESD design	43	D21, D22 change to SCA00000U10 and stuff D16, D17 change to SC300002C00 and stuff	06/25	SIT
44	HW design	14	Cardreader change port from port17 to port11 Lan change port from port18 to port12	07/10	SIT2
45	RF design	40	add CLIP116 for RF request	07/14	SIT2
46	HW design	41	LED1 change to PULL HIGH to +3VLP	07/27	SIT2
47	EMI design	36	CL170, RL61, CL169, DL1 change to EMI@	08/11	SVT
48	EC design	38	add R832 for no KBL function	08/11	SVT
49	EC design	40	R201, Q2, R202, Q1, C214 change to KBL@	08/11	SVT

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2015/02/06

Page 57

PU1601 change power sloution from SY8003D to SY198DQNC

Page 52

PR906 change from 45.3 +-1% 0402 to 100 +-1% 0402

Page 54

Add PC1337(S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9)

Page 56

PR1519,PR1532,PR1550 change from 1 +-1% 0402 to 1 +-1% 0201

PR1527 change from 100K +-5% 0402 to 100K +-5% 0201

PR1501,PR1502,PR1504,PR1508,PR1510,PR1516,PR1517,PR1518,PR1520,PR1529,PR1530,PR1531,PR1548,PR1549,PR1552 change from 10K +-5% 0402 to 10K +-5% 0201

2015/02/06

Page 47

PR412 change from 10_0402_1% to 0_0402_5%

Page 46

PR319 change from 10K_0402_1% to 100K_0402_1%

PR323 change from 12K_0402_1% to 120K_0402_1%

PR322 change from 10K_0402_1% to 0_0402_5%

Page 48

PC502 change from 0.22U_0402_10V6K to 0.1U_0402_25V6

PR501 change from 2.2_0402_1% to 0_0402_5%

Page 56

PR1554 change from 887 +-1% 0402 to 1.05K +-1% 0402

2015/03/16

Follow Power module design.

Page 46

PR328 change to non-mount

PC316 change from 2.2U_0805_25V6K to 2.2U_0603_16V6K

Page 48

PR501 change from 0_0402_5% to 2.2_0603_5%

PC502 change from 0.1U_0402_25V6 to 0.1U_0603_25V7K

Add PR513(5.1_0603_5%)

PC514 & PC515 change from 1U_0603_10V6K to 1U_0402_10V6K

2015/04/10

Modify for ADP_ID circuit

Page 44

Add PR107(0_0402_5%)

PQ101 , PR103 & PR104 change to non-mount

Modify for ADP_I circuit

Page 45

PR206 & PR208 change to non-mount

Change to 0 ohm R-short for part count reduce

Page 46

PR322 change to 0 ohm-short pad

Page 47

PR412 change to 0 ohm R-short

Page 53

PR1005, PR1006, PR1012, PR1015, PR1021 & PR1022 change to 0 ohm R-short

Consider power budget, It can change CHOKE size to 2520.

Page 51

PL801 change to 1UH +-20% 2.3A 2.5X2X1.2
FERRITE(SH000011S00)

3 cell battery design can reduce lpcs bead in VGA CORE

Page 56

Delete PL1502

2015/04/14

For CPU transient fine-tune

PC904 change from 0.039U_0603_25V7(SE00000A780) to .01U 50V K X7R 0402(SE074103K80)

PR902 change from 1K_0402_1%(SD034100180) to 12K_0402_1%(SD034120280)

PR913 change from 19.6K_0402_1%(SD000003580) to 47.5K_0402_1%(SD034475280)

PR912 change from 8.45K_0402_1%(SD000000680) to 19.1K_0402_1%(SD034191280)

PR920 change from 34.8K_0402_1%(SD034348280) to 35.7K_0402_1%(SD000007000)

PC901 change from 1000P_0402_50V7K(SE074102K80) to 2200P_0402_50V7K(SE074222K80)

PR910 change from 1K_0402_1%(SD034100180) to 2.32K_0402_1%(SD00000WS80)

PR933 change from 22.6K_0402_1%(SD034226280) to 23.7K_0402_1%(SD034237280)

PR935 ,PR939 change from 1K_0402_1%(SD034100180) to 590_0402_1%(SD00000C080)

PR934 change from 3.3K_0402_1%(SD00000GW80) to 4.7K_0402_1%(SD034470180)

PC918 ,PC922 change from 2200P_0402_50V7K(SE074222K80) to 3300P_0402_50V7K(SE074332KL0)

PR966 change from 52.3K_0402_1%(SD034523280) to 54.9K_0402_1%(SD00000H880)

PR964 change from 42.2K_0402_1%(SD034422280) to 44.2K_0402_1%(SD034442280)

PR940 change from 3.3K_0402_1%(SD00000GW80) to 4.12K_0402_1%(SD034412180)

For sourcer request,modify P/N

PC1001,PC1006,PC1013,PC1017,PC1029,PC1030 change from SE000005210(0.22U 25V K X7R 0603) to SE000005280(0.22U 25V K X7R 0603)

PC602 ,PC802 change from SE000008L80(22U 6.3V M X5S 0805 H1.25) to SE00000M000(22U 6.3V M X5R 0603)

PC203,PC204,PC312,PC402 change from SE075103K80(.01U 25V K X7R 0402) to SE074103K80(.01U 50V K X7R 0402)

PC505 ,PC506 change from SE093106K80(10U 6.3V K X5R 0805 H1.25) to SE000005T80(10U 6.3V M X5R 0603 H0.8)

PC1007,PC1008,PC1018,PC1020,PC1031,PC1032 change from SE107225KL0(2.2U 6.3V K X5R 0603) to SE000008880(2.2U 6.3V M X5R 0402)

to avoid leakage current at +1V_VCCST.

PR932 change to non-mount

Base on test result,reduce CPU output cap.

PC927 change to non-mount

PC1103 ,PC1105 ,PC1106 change to non-mount

PC1117 ,PC1113 ,PC1116 ,PC1109 change to non-mount

PC1146,PC1147,PC1148,PC1149 change to mount

For HW request,modify power sequence.

PC517 change from SE102104K00(0.1U_0402_10V7K) to SE074102K80(1000P_0402_50V7K)

PC1401 change from SE076104K80(0.1U_0402_16V7K) to SE074102K80(1000P_0402_50V7K)

VGA CORE component over heat issue,change to AON6970 to reduce power loss.

PQ1501 ,PQ1502 ,PQ1503 change from SB00000XJ10 (AON6932A 2N DFN5X6-8) to SB000010K00(AON6970 2N DFN5X6D)

2015/04/30

Force VGA core work in 3-phase CCM mode

Add PR1524 (10K +-1% 0201)

Add snubber and 6.8pF cap for EMI and RF request

Add PR405 & PR411 (4.7_1206_5%)

Add PC412 & PC428 (680P_0603_50V7K)

Add PR1007,PR1008,PR1016,PR1014,PR1023,PR1024 (4.7_1206_5%)
Add PC1009,PC1010,PC1021,PC1019,PC1033,PC1034(680P_0603_50V7K)

Add PC704(6.8P_0402_50V8C)

Add VGA VR11# protection circuit to VGA AC batt (CPU16.9)

Add PR1610(100K_0201_5%)

Add PQ1504(DMN65D8LDW-7_SOT363-6)

Modify for ADP_ID circuit

Delete PR107(0_0402_5%)

2015/06/01

Follow Power module design.

PR309 & PR310 change from 10 ohm to R-short

Reduce part count for 3S battery design

Delete PR221 and PR225

Reduce part count

PR904, PR909, PR916, PR921, PR923, PR924, PR925, PR929

, PR976, PR977, PR978 change to 0-ohm R-short

PR1514, PR1511 change to 0-ohm R-short

Base on power budget ,modify solution

PU1401 change to SYX196DQNC

2015/06/05

Reduce part count

PR313, PR317, PR320, PR511, PR1409, PR1605 change to 0-ohm R-short

Skylake RTC circuit modify

Add PR107(45.3K_0603_1%)

Add PR105 change from 1K_0603_5% to 1.5K_0603_5%

2015/06/08

Reduce part count

PR1003, PR1013, PR1020, PR1004, PR1011, PR1019 change to 0805 0-ohm R-short

PR314, PR404, PR410, PR704, PR1404, PR1522, PR1542

PR1604 change 0603 0-ohm R-short

EMI & RF request

Add PR325(4.7_1206_5%) and PC320(680P_0603_50V7K)

PR316 change from 0_0603_5% to 2.2_0603_5%

Reserve PC1615(6.8P_0402_50V8C)

2015/06/22

For RF noise issue

Change CPU cap location from PC1101 & PC1102 to PC1103 & PC1105

Delete PC1101 & PC1102

For CPU transient fine-tune

PR913 change from 47.5K_0402_1% to 48.7K_0402_1%

PR933 change from 23.7K_0402_1% to 23.2K_0402_1%

PC928 change from 1000P_0402_50V7K to 1200P_0402_50V7K

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