

Compal Confidential

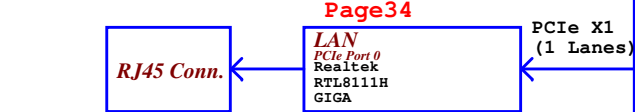
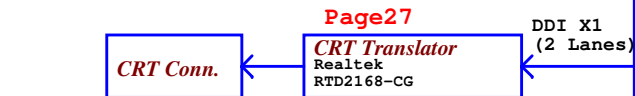
AIWZ0/AIWZ1
DIS M/B Schematics Document
Intel Boardwell U Processor with DDR3L
AMD Meso XT / Tropo XT2

2015-02-02

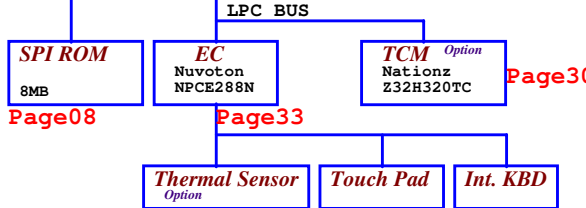
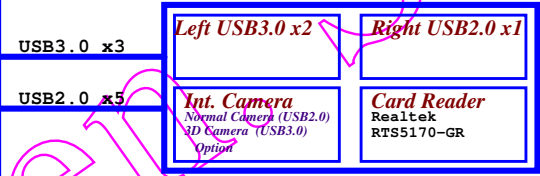
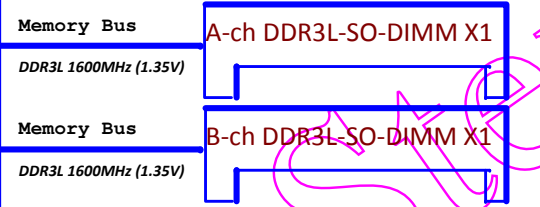
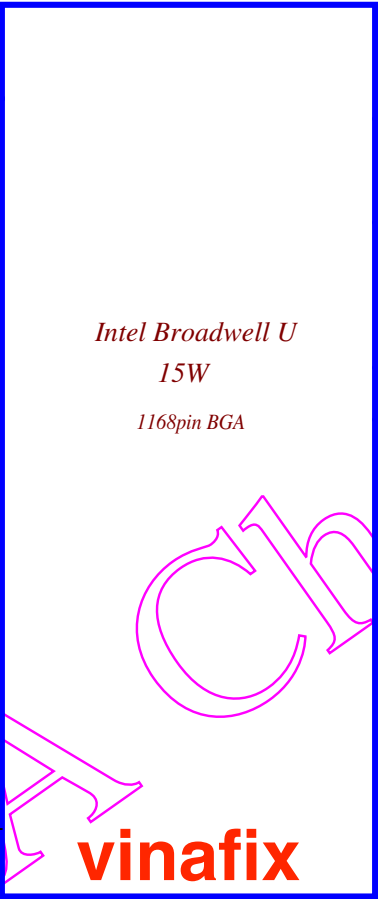
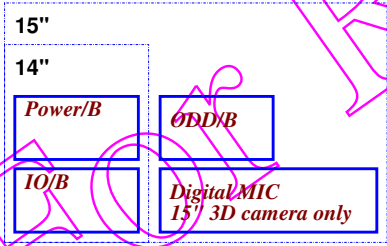
LA-C281P

REV : 1.0

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Sub-borad



Power Rails

power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +VCC_CORE +VGA_CORE +1.8VS +0.675VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011x	Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	Device	Address
DDR_JDIMM1	1010 000x A0h	Internal thermal sensor	0100 0001 41h
DDR_JDIMM2	1010 010x A4h		

SM Bus Control Table

	SOURCE	CRT	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
EC_SMB_CLK1	NPCE288	✗	✓	✗	✗	✗	✗	✗
EC_SMB_DA1	+3VALW	✓	+3VALW	✗	✗	✗	✗	✗
EC_SMB_CLK2	NPCE288	✓	✗	✗	✗	✗	✓	✓
EC_SMB_DA2	+3VS	+3VS	✗	✗	✗	✗	+3VS	+3VALW
PCH_SMB_CLK	PCH	✗	✗	✗	✓	✗	✗	✗
PCH_SMB_DATA	+3VALW	✓	✗	✗	+3VS	✗	✗	✗
PCH_SML0_CLK	PCH	✗	✗	✗	✗	✗	✗	✗
PCH_SML0_DATA	+3VALW	✓	✗	✗	✗	✗	✗	✗
SML1_CLK	PCH	✓	✗	✗	✗	✗	✓	✗
SML1_DATA	+3VALW	+3VS	✗	+3VS	✗	✗	+3VGS	✗

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)USB3.0
		1	USB Port (Left Side)USB3.0
	UHCI1	2	Sub Board
		3	CardReader
	UHCI2	4	Touch Screen
		5	Camera
EHCI1	UHCI3	6	Bluetooth (NGFF)
		7	
	UHCI4	8	
		9	
	UHCI5	10	
		11	
EHCI1	UHCI6	12	
		13	

BDW_CPU

UC1
SA000089A60 17-5500U
S IC FH8065801620004 SR23W F0 2.4G C38!
17_5500@

UC1
SA000089970 15-5200U
S IC FH8065801620204 SR23Y F0 2.2G C38!
15_5200@

UC1
SA000089880 13-5010U
S IC FH8065801620406 SR23Z F0 2.1G C38!
13_5010@

UC1
SA000083EH0 13-5005U
S IC FH8065801884006 SR244 F0 2G C38!
13_5005@

PCB

ZZZ
DA218K00101
PCB AIWZ0 LA-C281P LS-C281P/C282P 02
Z14@
PCB AIWZ0 LA-C281P LS-C281P/C282P 02

ZZZ
DA218J00101
PCB AIWZ1 LA-C281P LS-C281P/C282P/C283P/C285P/C286P 02
Z15@
PCB AIWZ1 LA-C281P LS-C281P/C282P/C283P/C285P/C286P 02

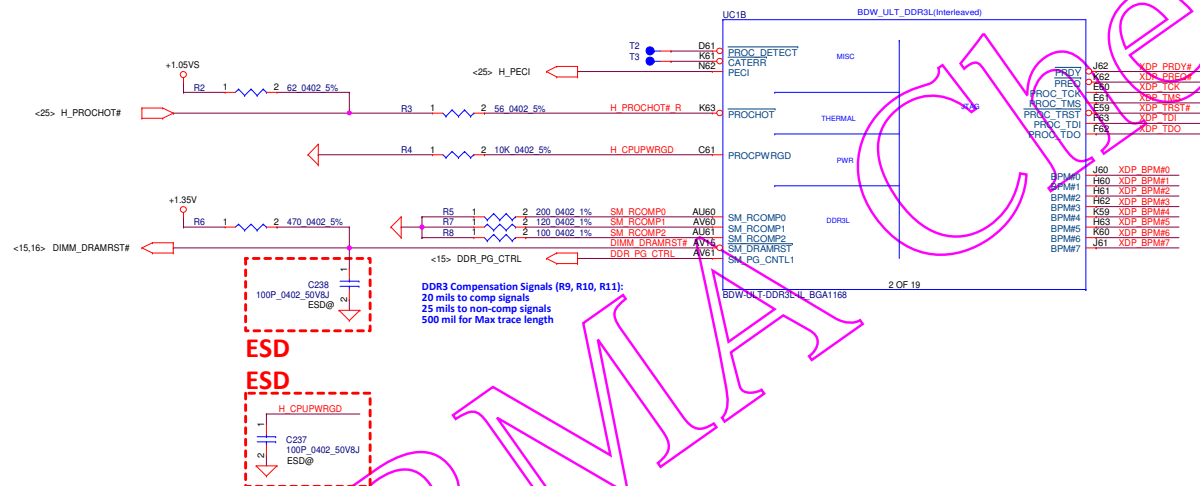
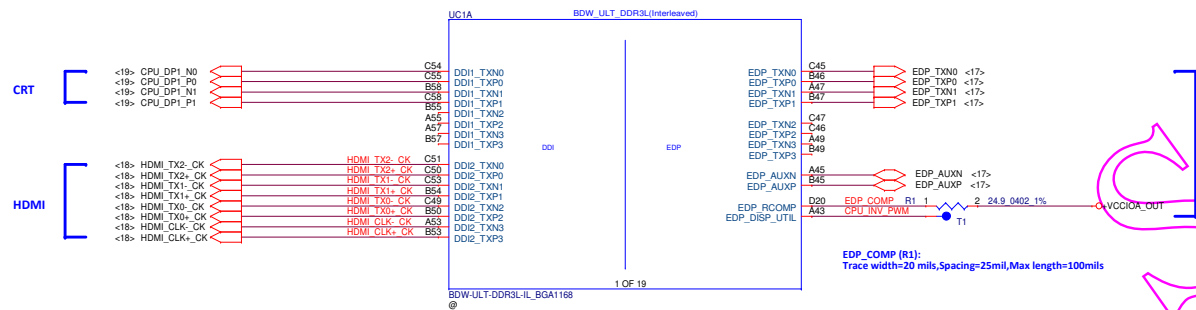
BOM Structure Table

Item	BOM Structure
AIWZ0 (14")	Z14@
AIWZ1 (15")	Z15@
AIWZ0 (17")	Z17@
LAN Switch mode	SWITCH@
LAN RTL811GS-CG	8111GLDO@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NOISCT@
For Green CLK	GCLK@
For No Green CLK	NOGCLK@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
For system DIS	PX@
For TROP DIS pop	DIS@
For TROP DIS unpop	@DIS@
For UMA	UMA@
3D Camera	3DCMOS@
Camera	CMOS@
HDMI	HDMI@
NO keyboard backlight	NOKBL@
Keyboard backlight	KBL@
HDMI Royalty	45@
Connector	ME@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
pop component for EMI	EMI@
pop component for ESD	ESD@
Un-pop for TPM	TPM@
pop for TPM	NOTPM@
VRAM identify	X76@
For TROP function	TROP@
ADB function	ADB@
NO ADB function	NOADB@
CPU_SA000083E30	QGZ3@
CPU_SA000083C10	QH17@
CPU_SA00007AM00	QFSY@
CPU_SA000083A10	QH15@
CPU_SA000083D30	QH18@
CPU_SA00007UG00	QGHA@
CPU_SA00007UH00	QGH@
CPU_SA00007U900	QGH9@

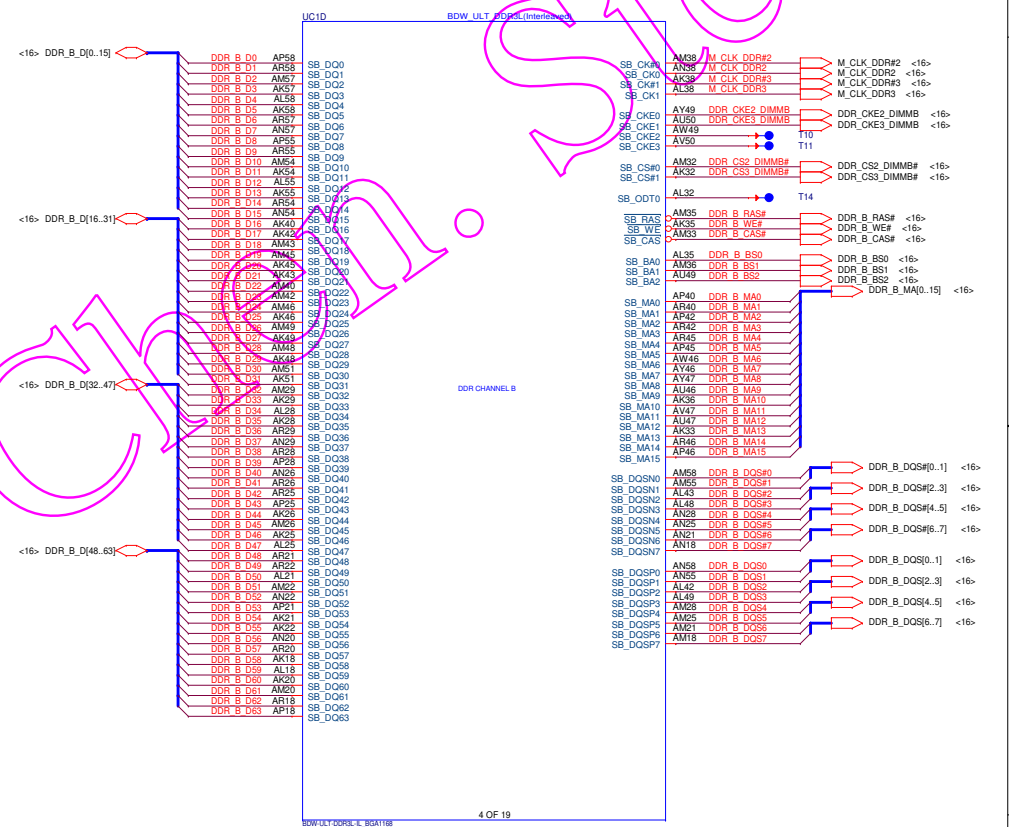
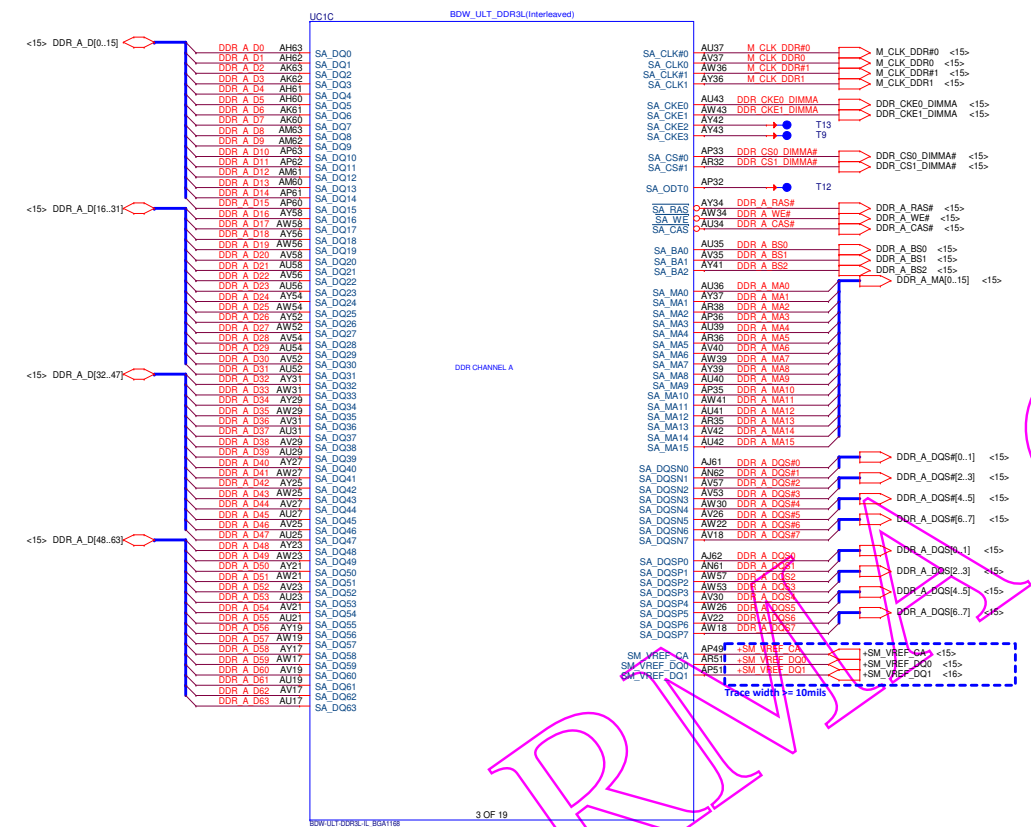
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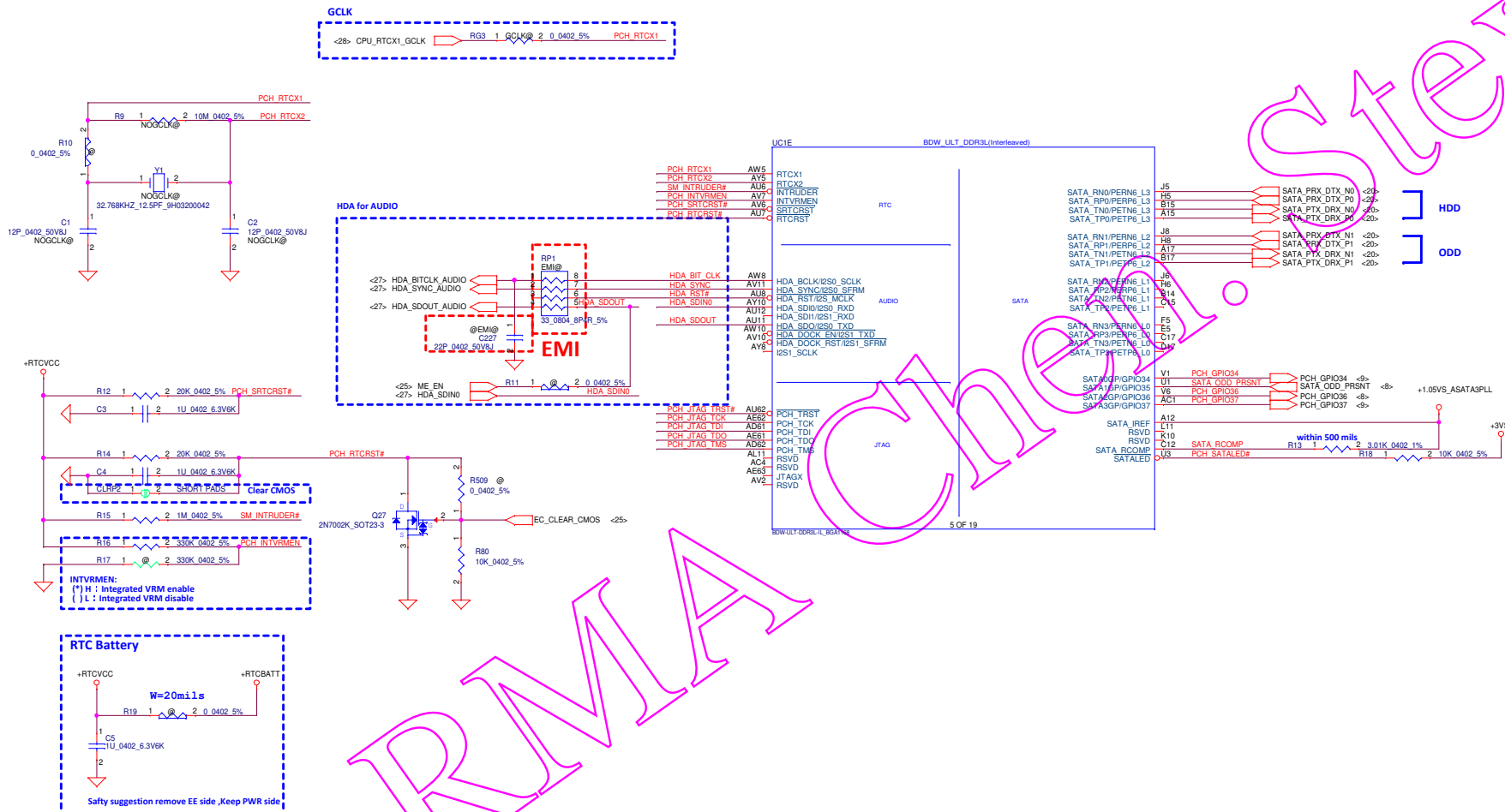
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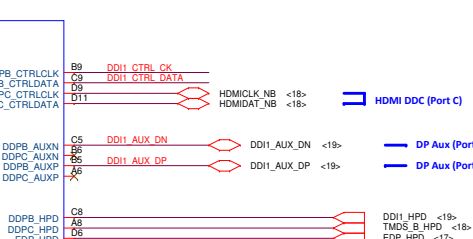
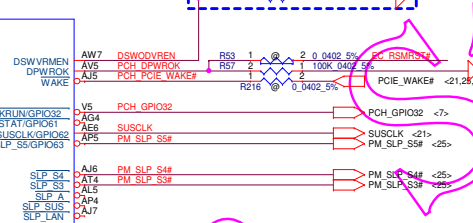
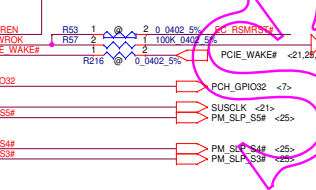
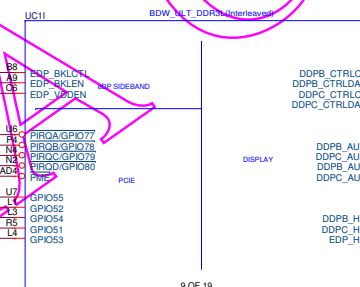
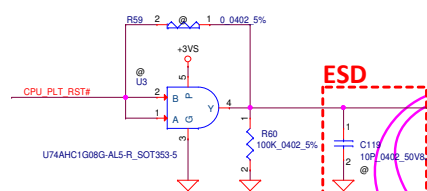
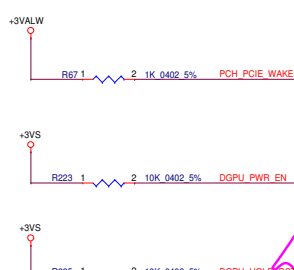


Interleaved Memory

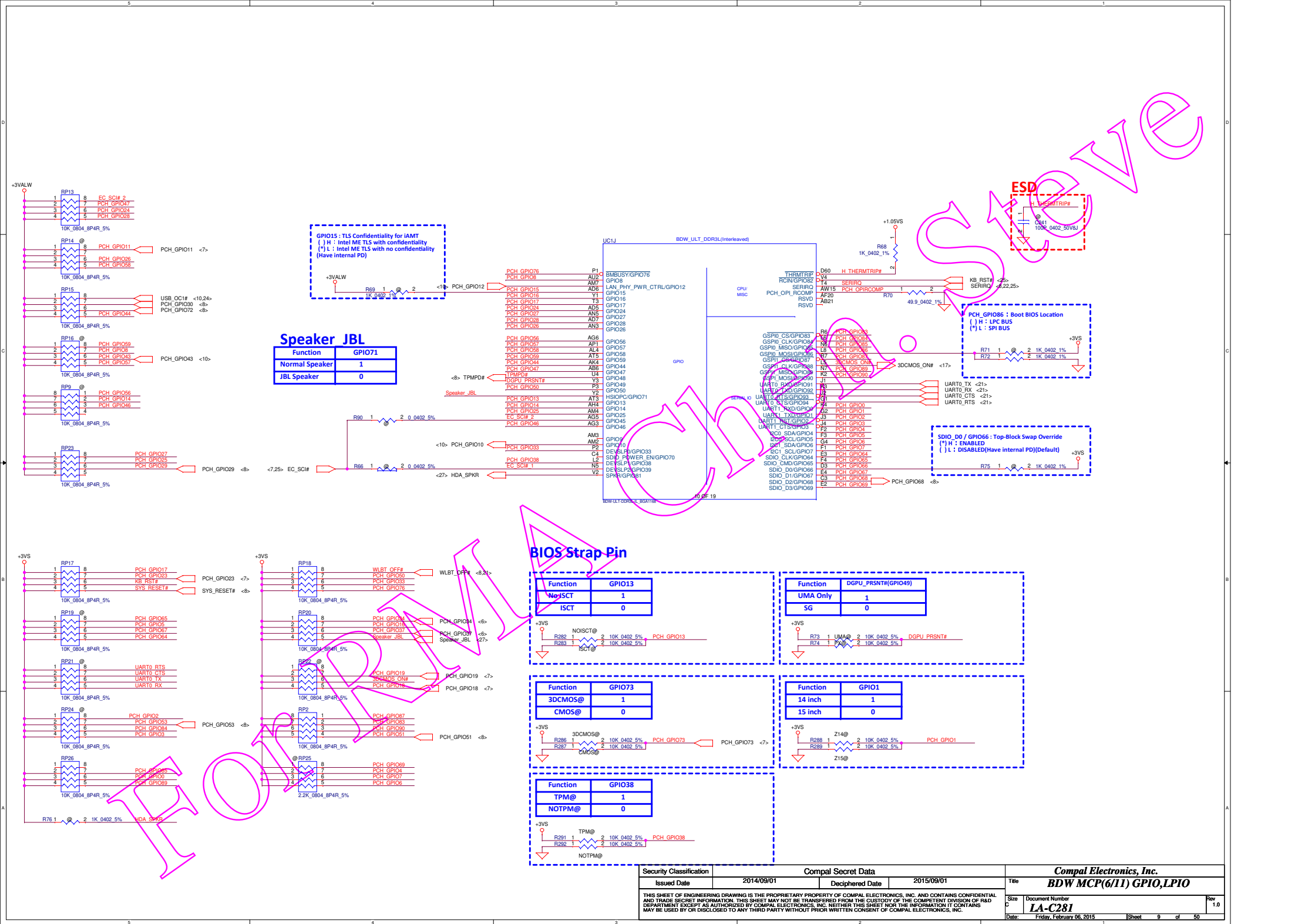


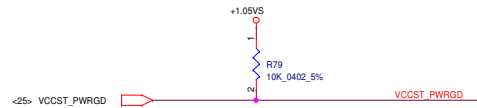
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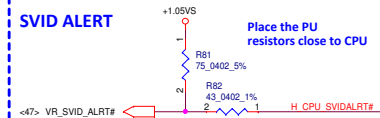


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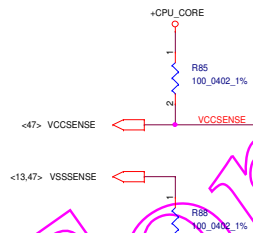
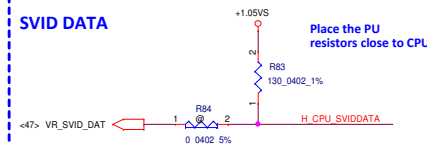




SVID ALERT



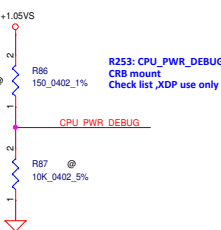
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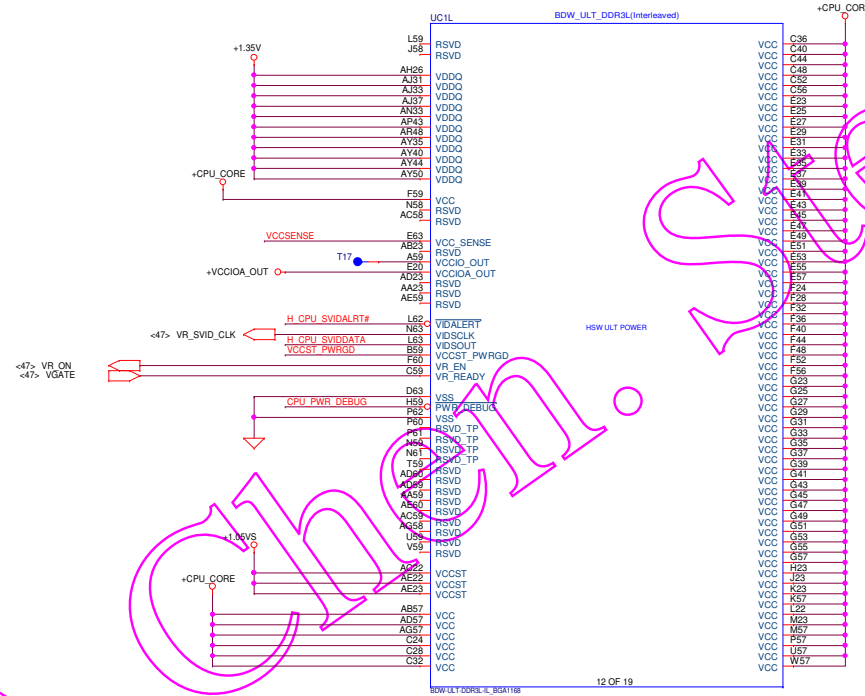
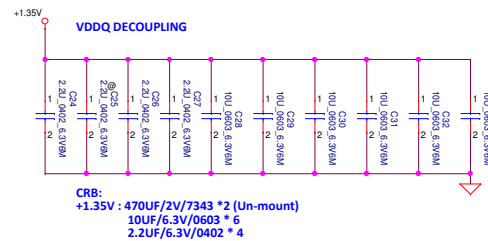
PU resistor should be close to CPU



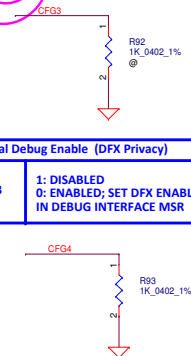
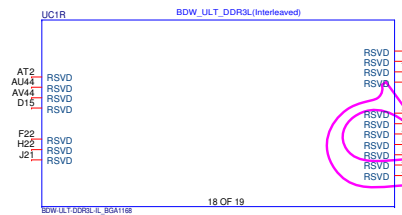
PD resistor should be close to CPU



VDDQ DECOUPLING

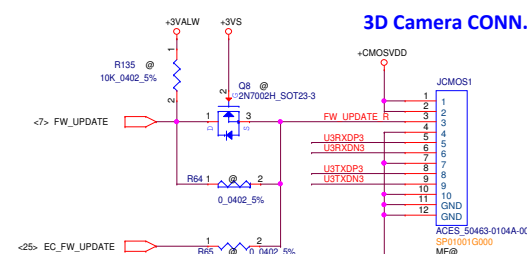
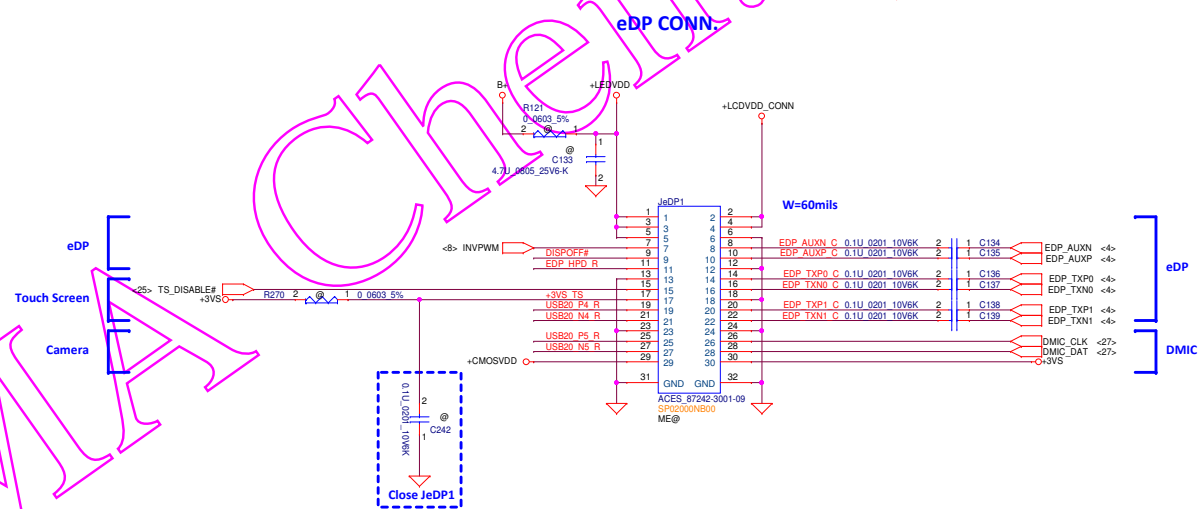
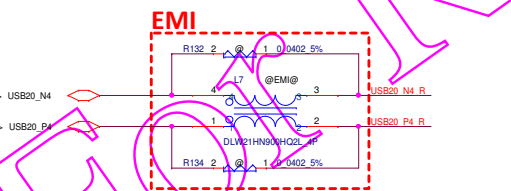
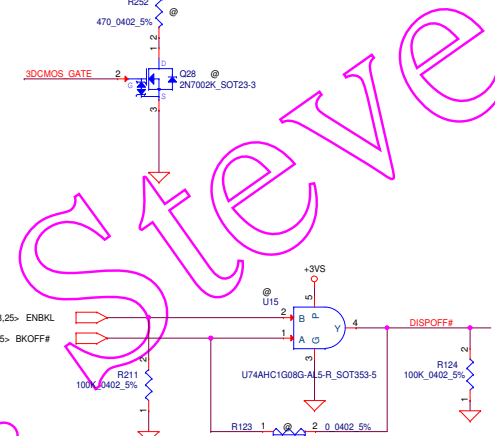
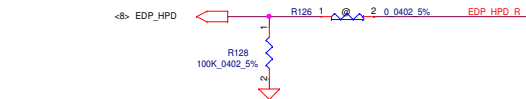


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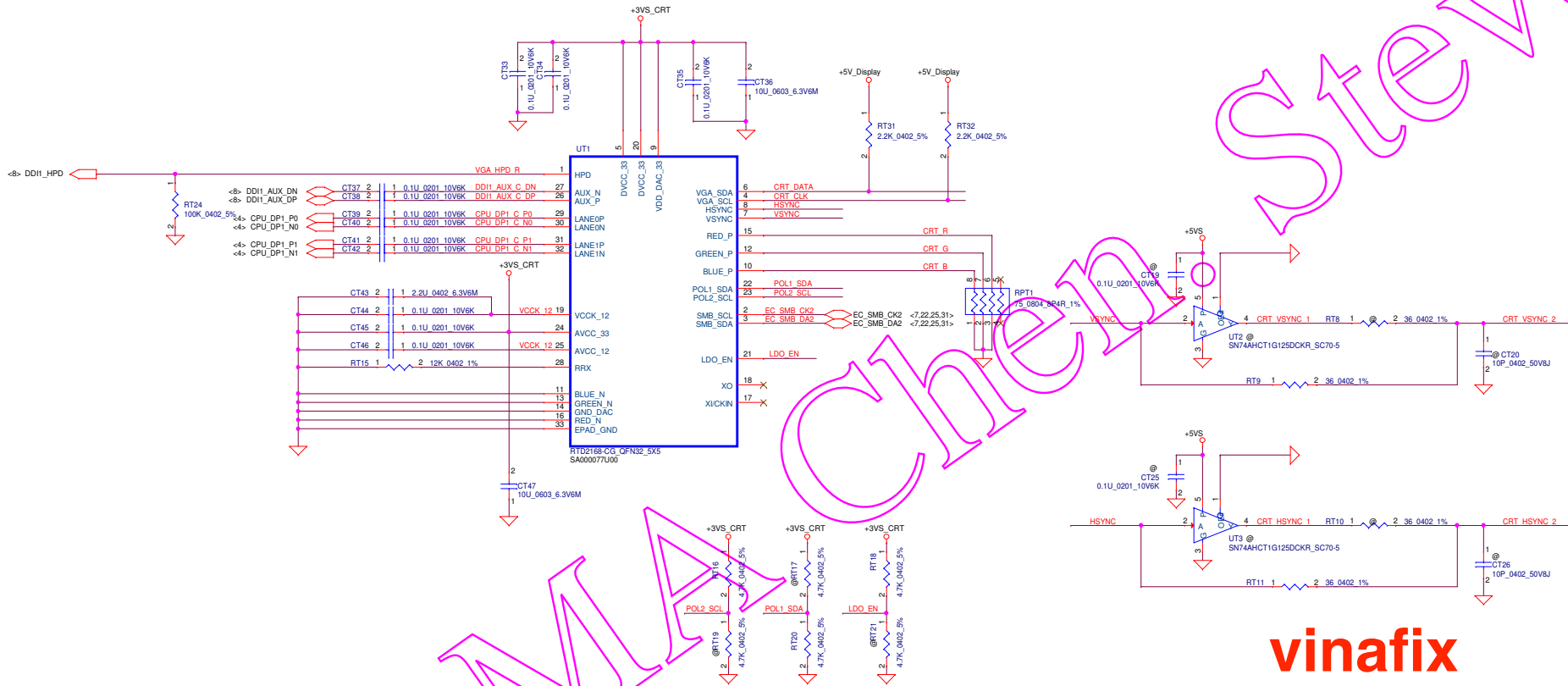
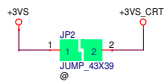


Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

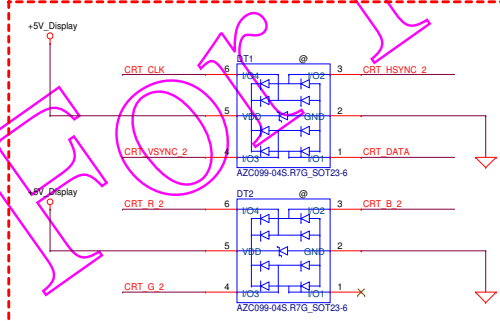
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



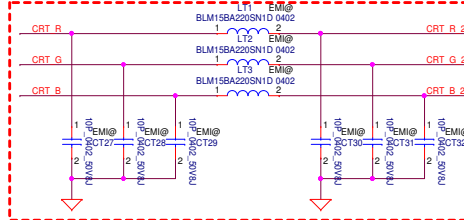
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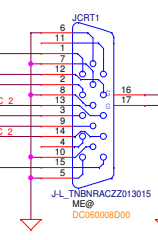
ESD



EMI

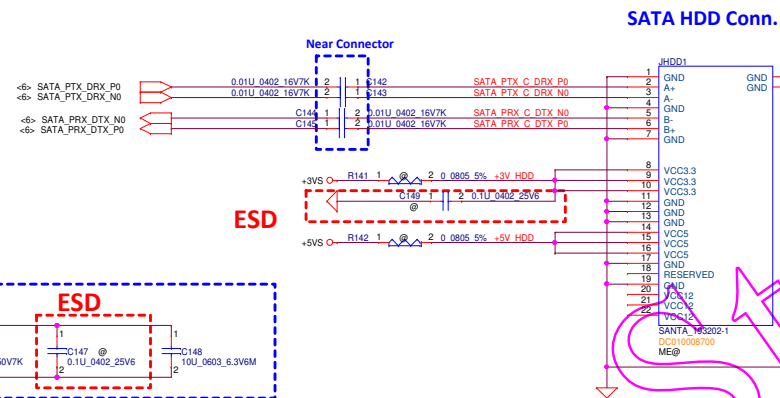


CRT

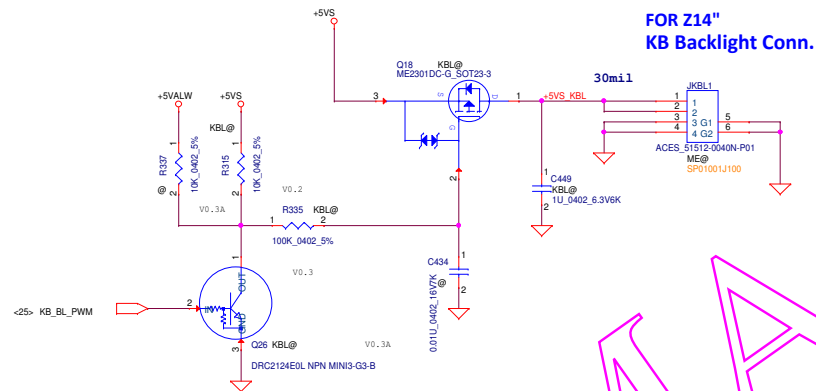


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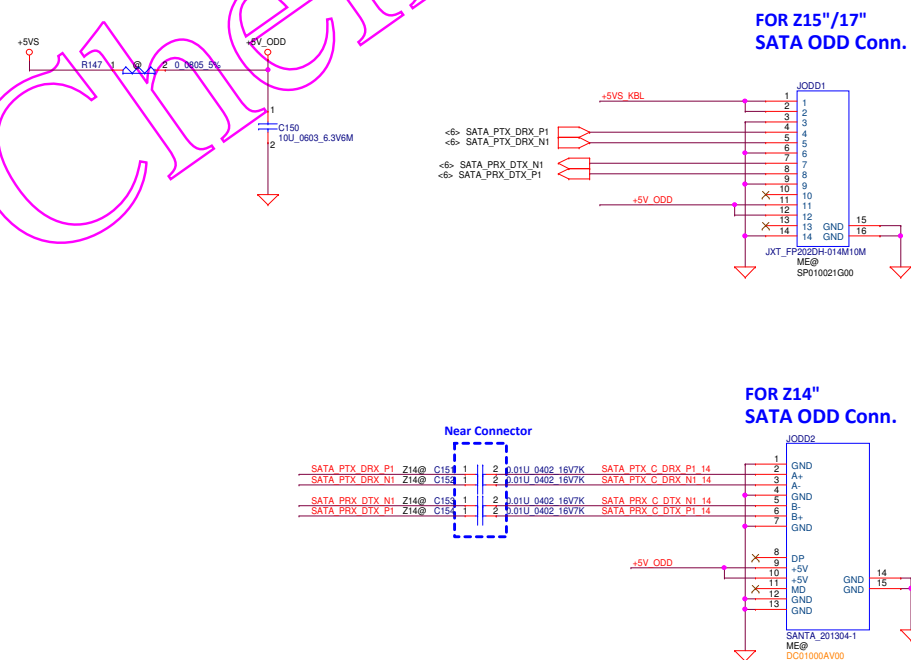
HDD



KB Backlight

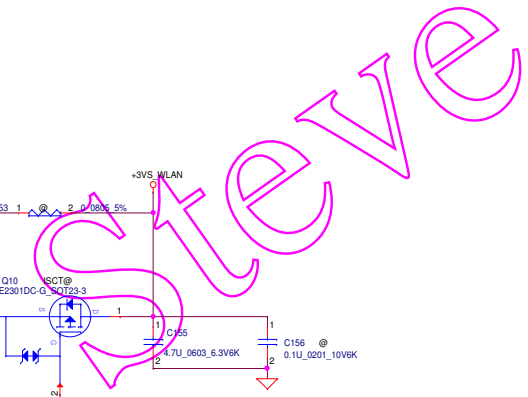


ODD



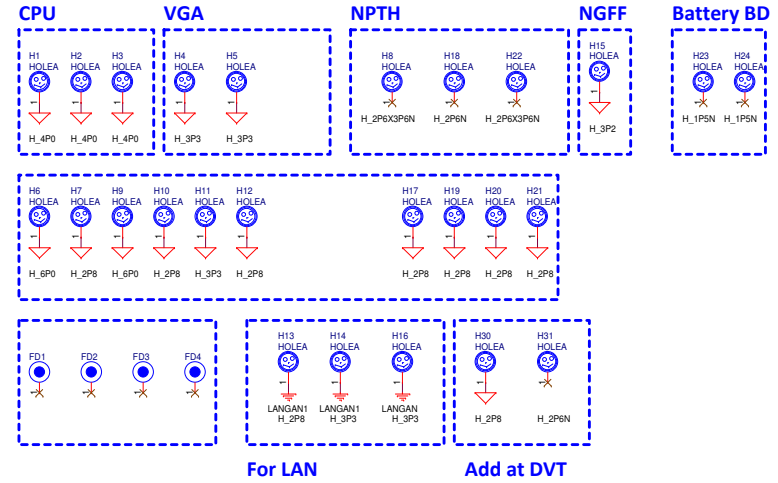
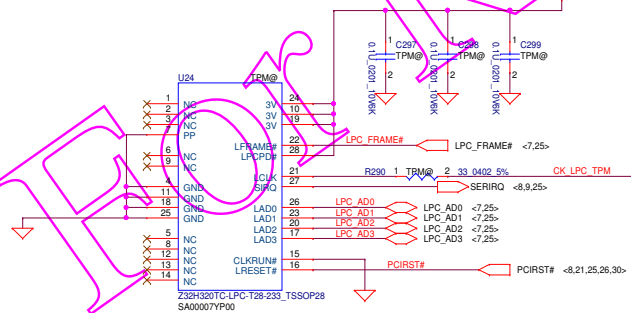
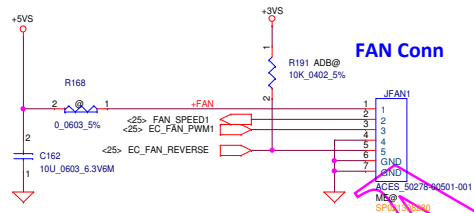
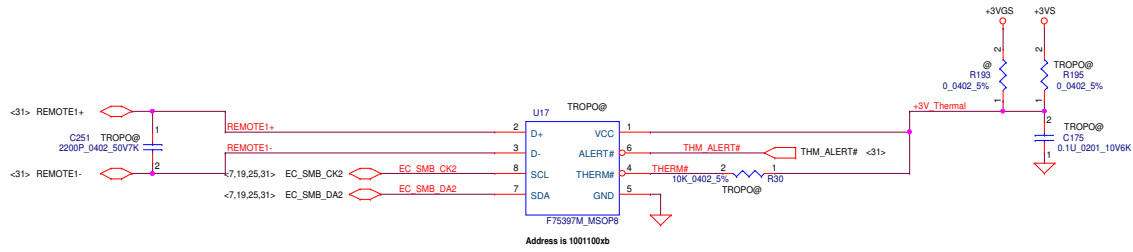
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FORMER



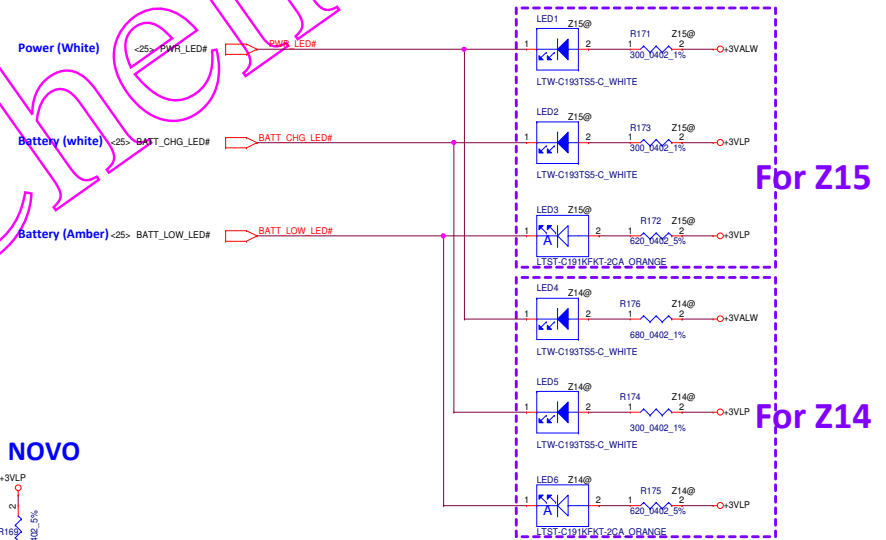
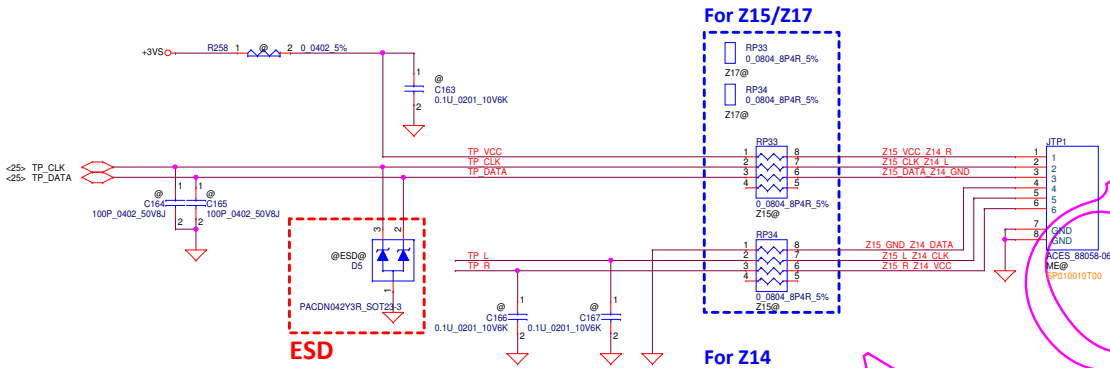
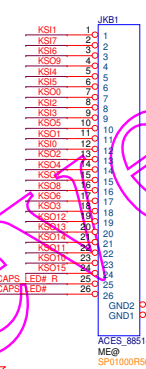
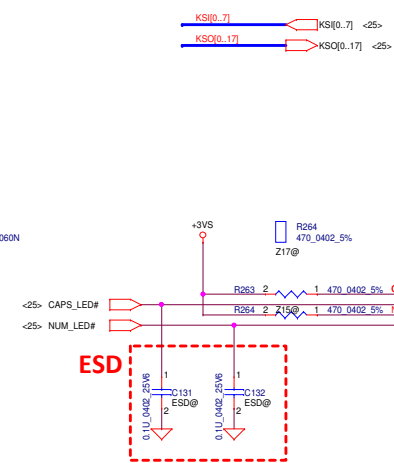
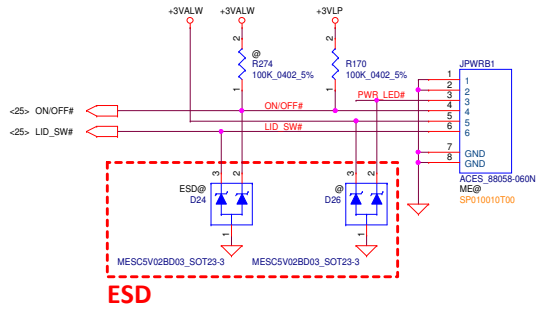
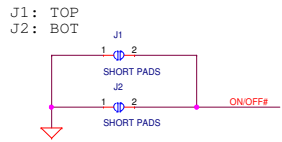
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				Date:	Friday, February 06, 2015
				Sheet	21 of 50

2 Channel



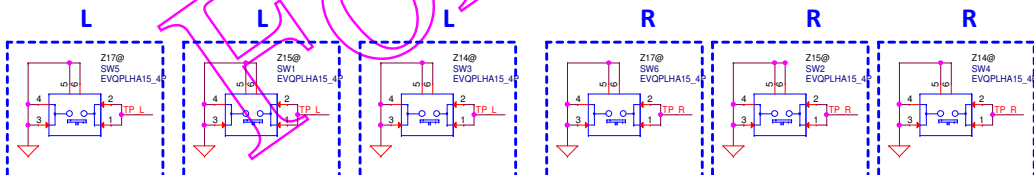
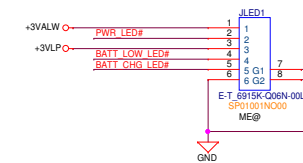
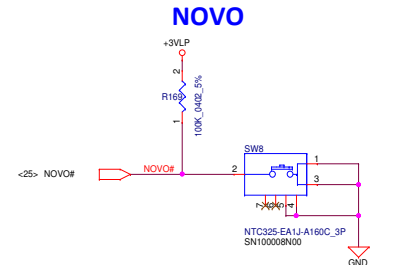
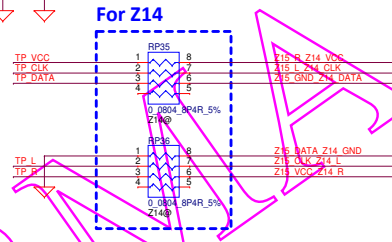
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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title	Fintek-Thermal IC/FAN/screw	
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				Date: Friday, February 06, 2015	Sheet	22 of 50

vinafix

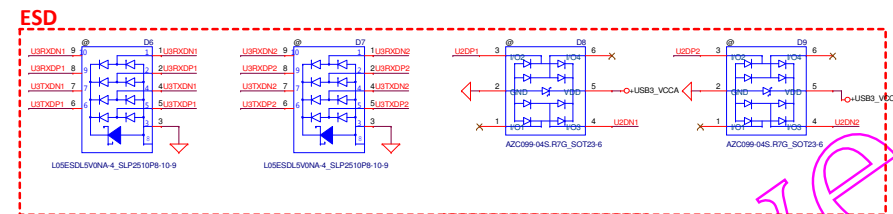
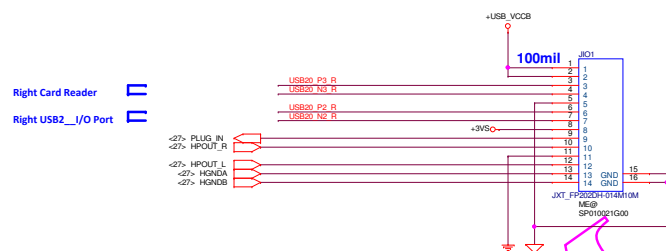


6	1	VCC
5	2	CLK
4	3	DAT
3	4	GND
2	5	L
1	6	R

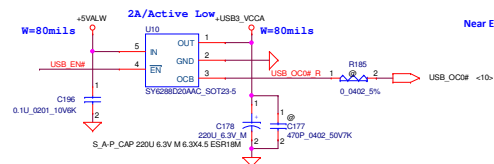
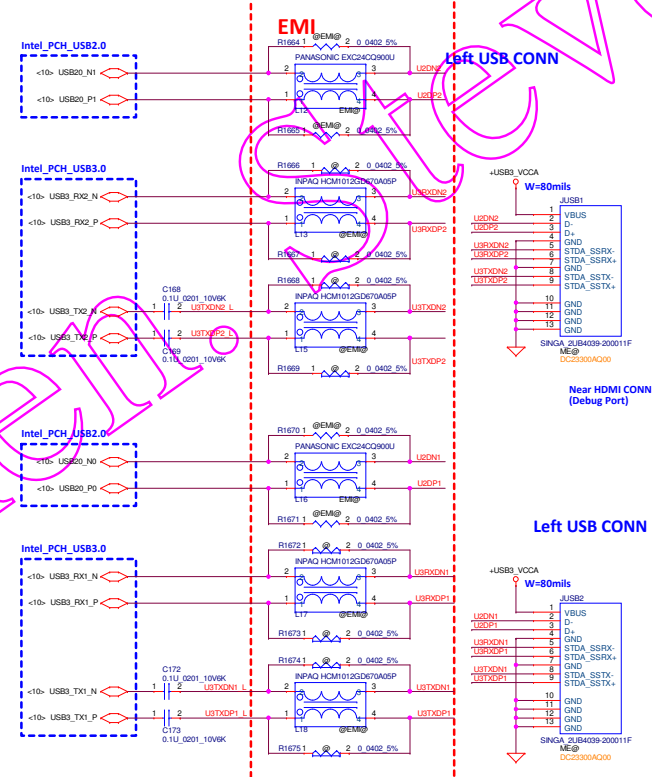
MB TP module




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2014/09/01		2015/09/01		LA-C281	
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Date				Friday, February 06, 2015	23 of 50



USB3.0 Port



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			Sheet 24	of 50

For Review

Compal Secret Data

EMI

CG9 no stuff any of component

CG8 just can use 4.7pF~33pF

CG7 no stuff any of component

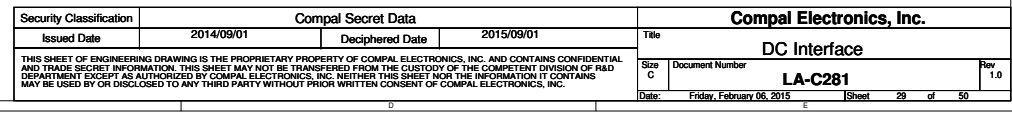
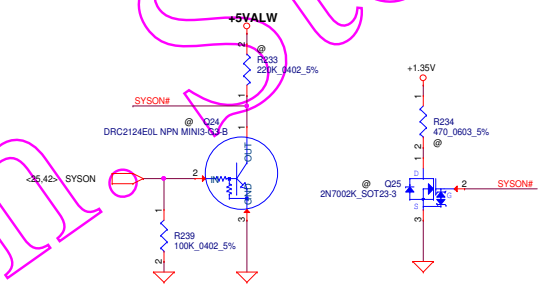
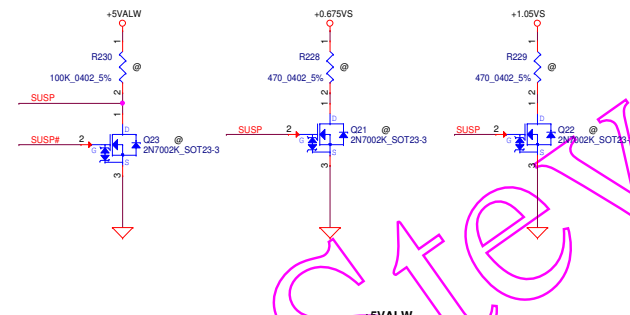
CPU_32.768KHz

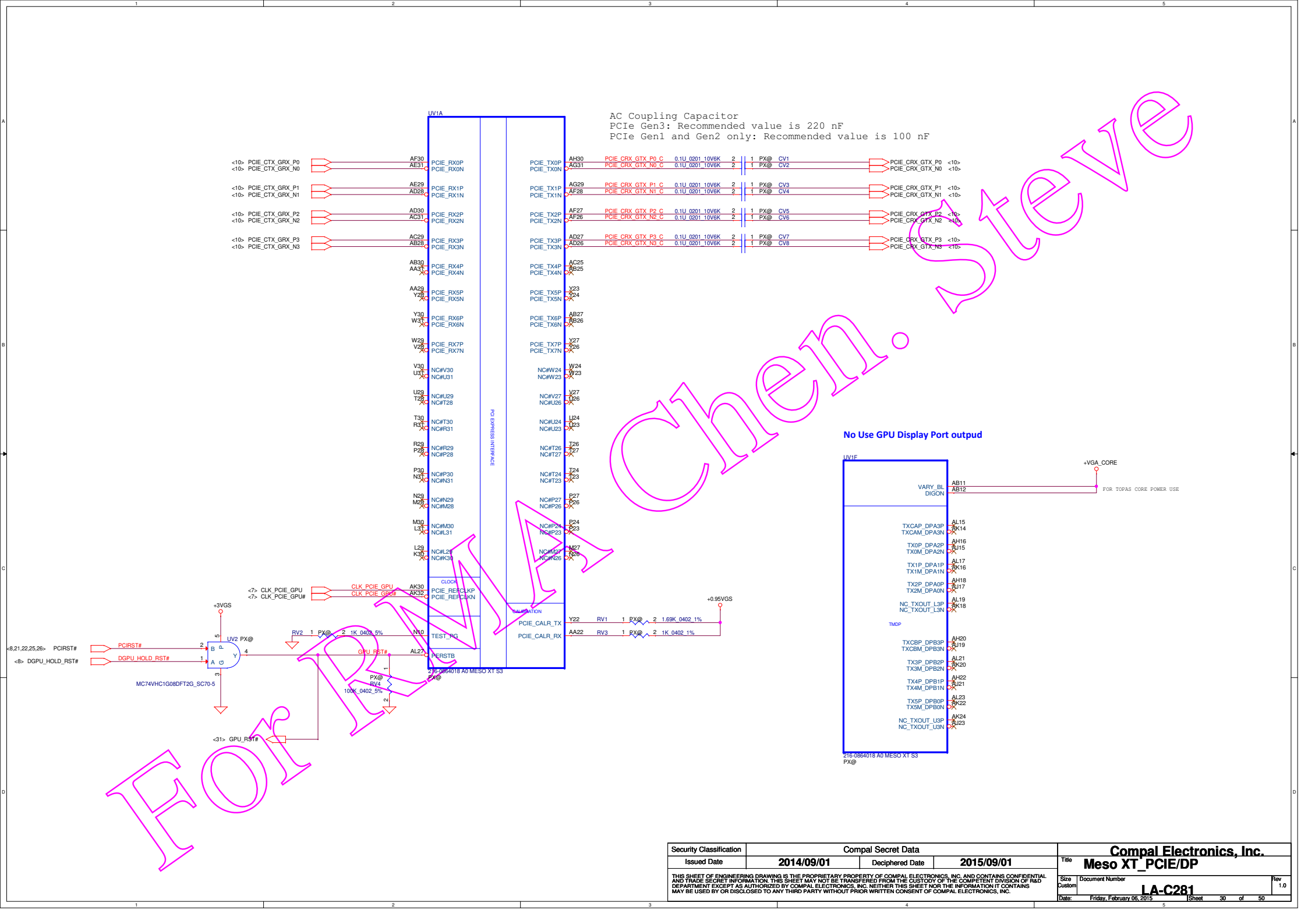
GPU_27MHz only for DIS

LAN_25MHz

CPU_24MHz

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				1.0





AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No Use GPU Display Port output

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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title	Meso XT_PCIE/DP
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				Date	Friday, February 06, 2015
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[illegible]

Diagram illustrating the power supply section for the AD9288, showing connections for +1.8VGS and +0.95VGS rails.

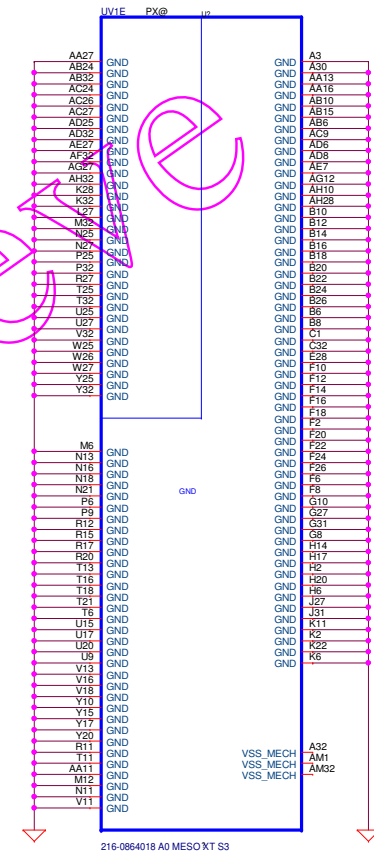
Power Supply Connections:

- +1.8VGS:** Connected to the top of CV22 and CV24. A 100k resistor (CV23) connects the top of CV22 to the top of CV24.
- +0.95VGS:** Connected to the bottom of CV28 and CV29. A 100k resistor (CV27) connects the bottom of CV28 to the bottom of CV29.

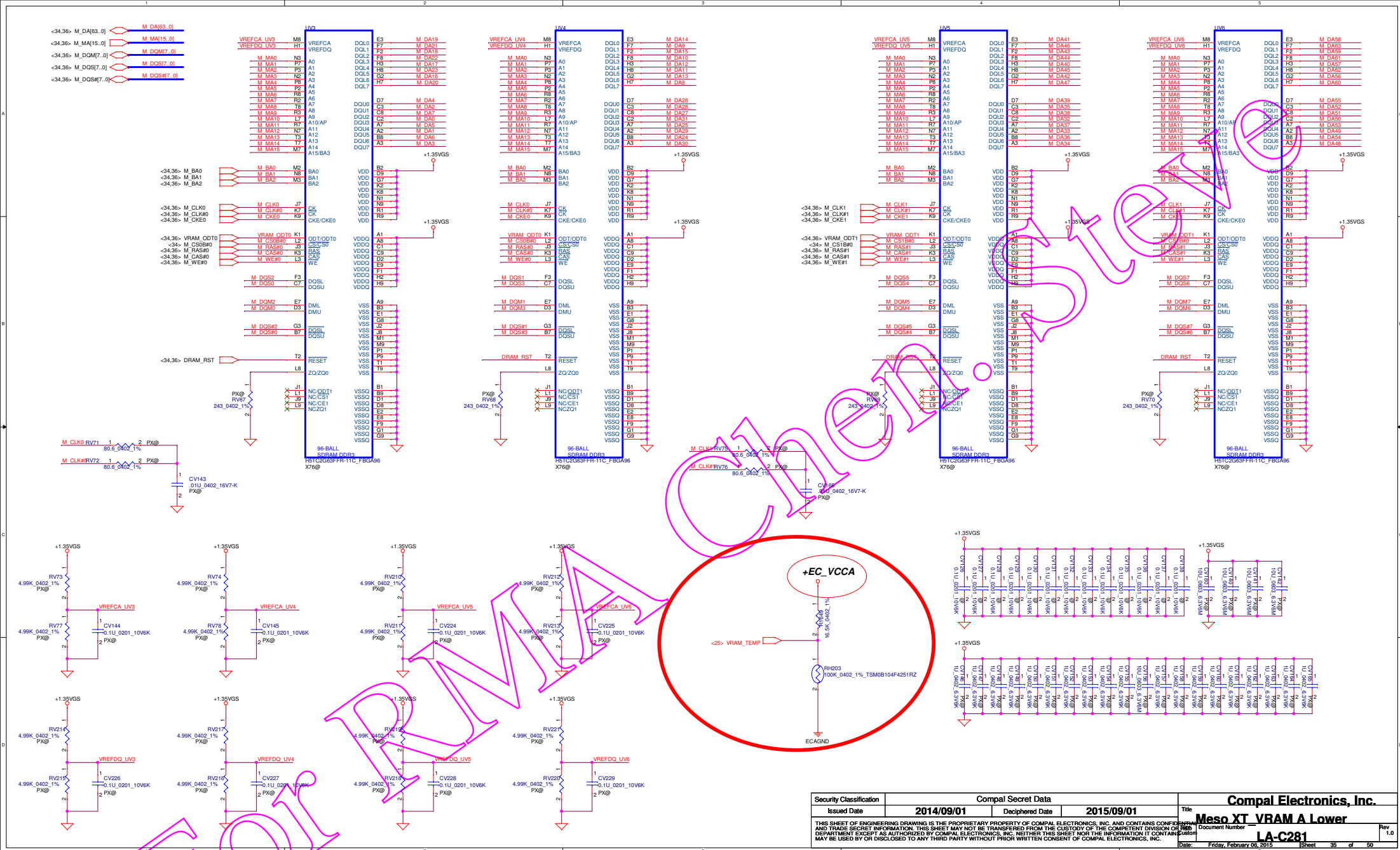
Pin Connections Table:

Pin	Signal	Connection
AG15	DP_VDDIRAG15	NC#AE11
AG16	DP_VDDIRAG16	NC#AF11
AF16	DP_VDDIRAF16	NC#AE13
AG17	DP_VDDIRAG17	NC#AF13
AG18	DP_VDDIRAG18	NC#AG8
AF17	DP_VDDIRAF17	NC#AG10
AD17	DP_VDDIRAD14	
AG20	DP_VDDC#AG20	NC#AF9
AG21	DP_VDDC#AG21	NC#AF1
AF22	DP_VDDC#AF22	NC#AF9
AG22	DP_VDDC#AG22	NC#AF9
AD19	DP_VDDC#AD14	
AG14	DP_VSSR	NC#AE1
AH14	DP_VSSR	NC#AE3
AM14	DP_VSSR	NC#AG1
AM16	DP_VSSR	NC#AG6
AM18	DP_VSSR	NC#AE6
AF23	DP_VSSR	NC#AF3
AG23	DP_VSSR	NC#AG9
AM20	DP_VSSR	NC#AF6
AM22	DP_VSSR	NC#AM5
AM24	DP_VSSR	NC#AM5
AF19	DP_VSSR	NC#AM5
AF20	DP_VSSR	NC#AG7
AE14	DP_VSSR	NC#AG11
AF17	DRAB_CALR	NC#AE10

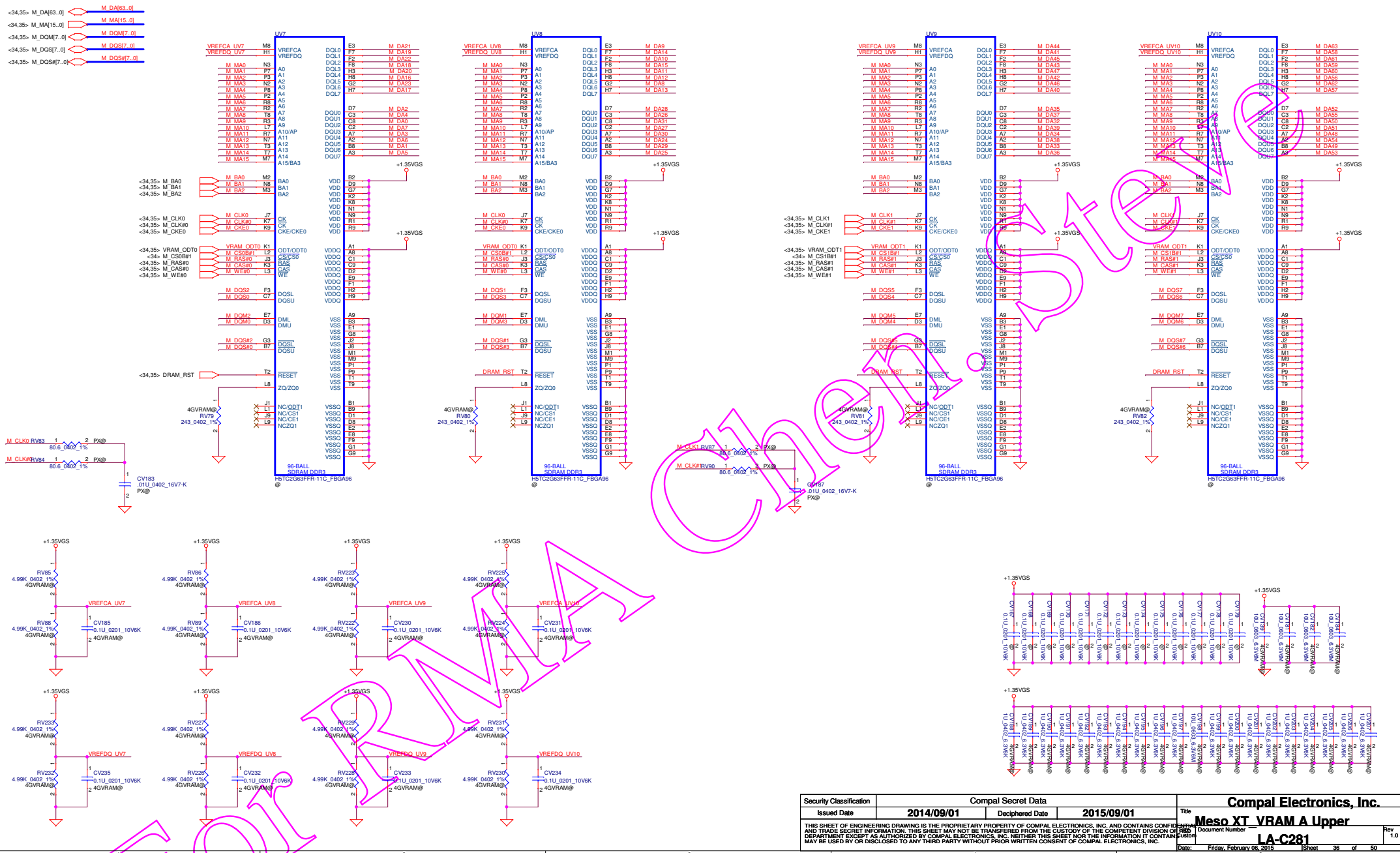
216-0864018 AD MESO XT[®] S3



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				LA-C281		
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			Document Number	LA-C281
Date	Friday, February 06, 2015	Sheet	35	of 50



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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Meso XT VRAM A Upper Document Number LA-C281	
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Date:			Friday, February 06, 2015	Sheet	38 of 50

Meso XT_VRAM_TRAP

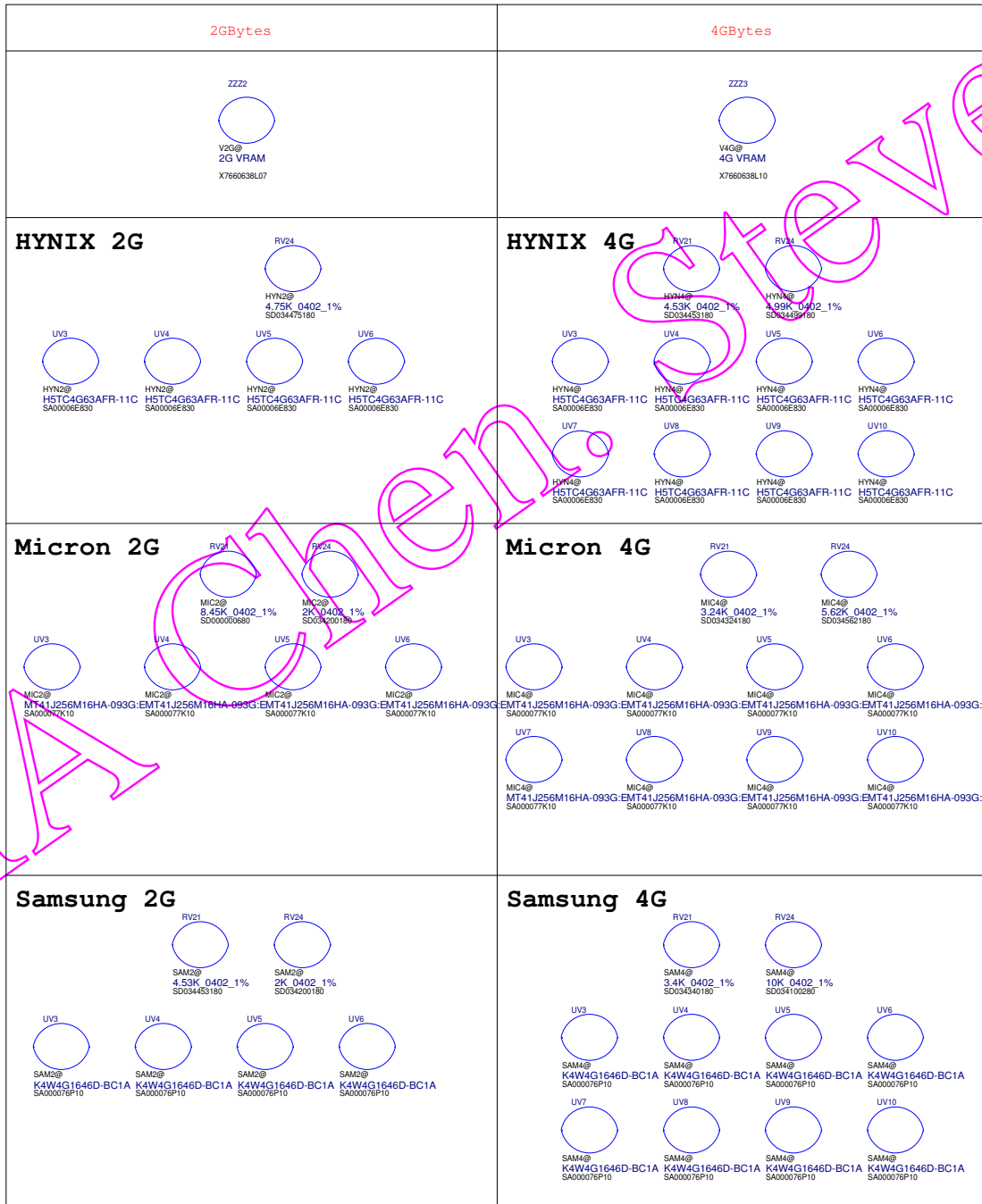
X76@

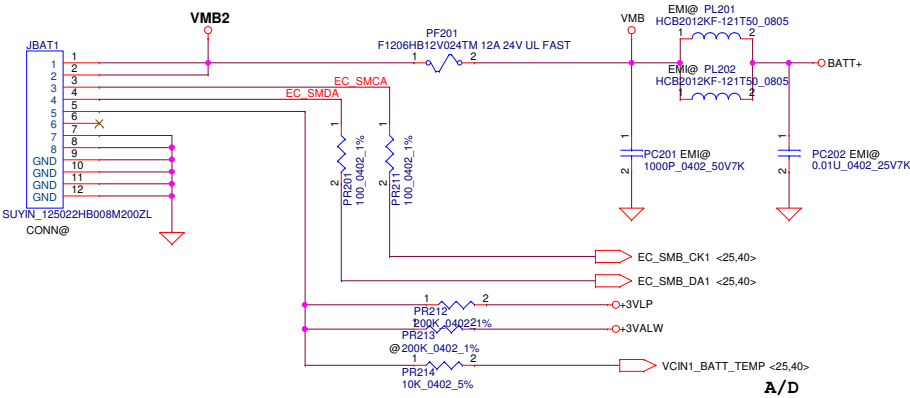
X76@

	Vendor	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
						RV21	RV24
2GBytes	UV3, UV4, UV5, UV6, UV7, UV8, UV9, UV10						
HYN2@	Hynix 2G SA00006E830 256Mx16 H5TC4G63AFR-11C	0	0	0	0	NC	4.75K
2GBytes	MIC2@	1	0	0	1	8.45K	2K
2GBytes	SAM2@	2	0	1	0	4.53K	2K
		3	0	1	1	6.98K	4.99K
4GBytes	HYN4@	4	1	0	0	4.53K	4.99K
4GBytes	MIC4@	5	1	0	1	3.24K	5.62K
4GBytes	SAM4@	6	1	1	0	3.4K	10K
		7	1	1	1	4.75K	NC

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

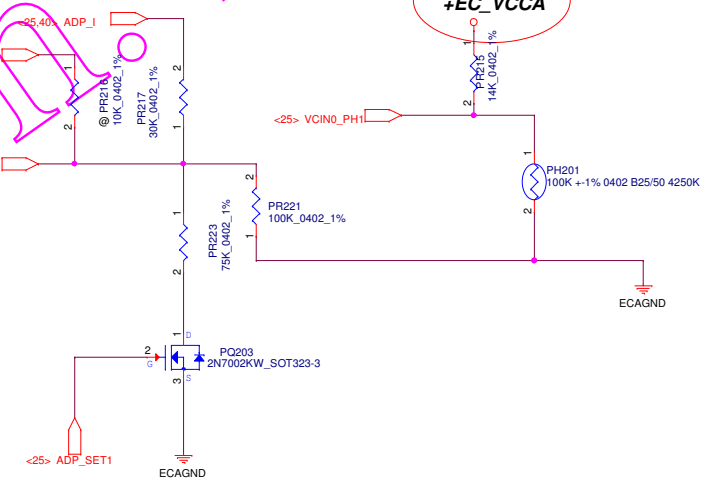




PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

Steve

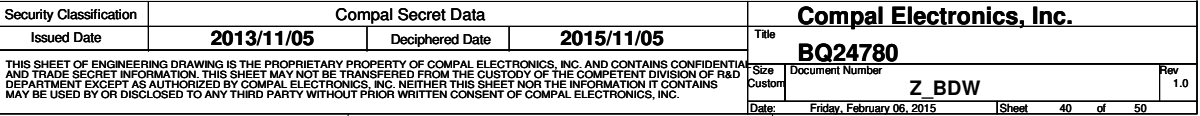
20120314
 Change to +EC_VCCA from +3VLP



	ADP_SET1	ADP_SET2
45W adapter	0	0
65W adapter	1	0
90W adapter	0	1
135W adapter	1	1

135W: 150W active, 135W recovery
90W : 120W active, 90W recovery
65W : 85W active, 65W recovery
45W : 65W active, 45W recovery

For RMA



SY8208B_V2.mdd

Change 3V5V_EN to 3VALW_EN

ENLDO_3V5V

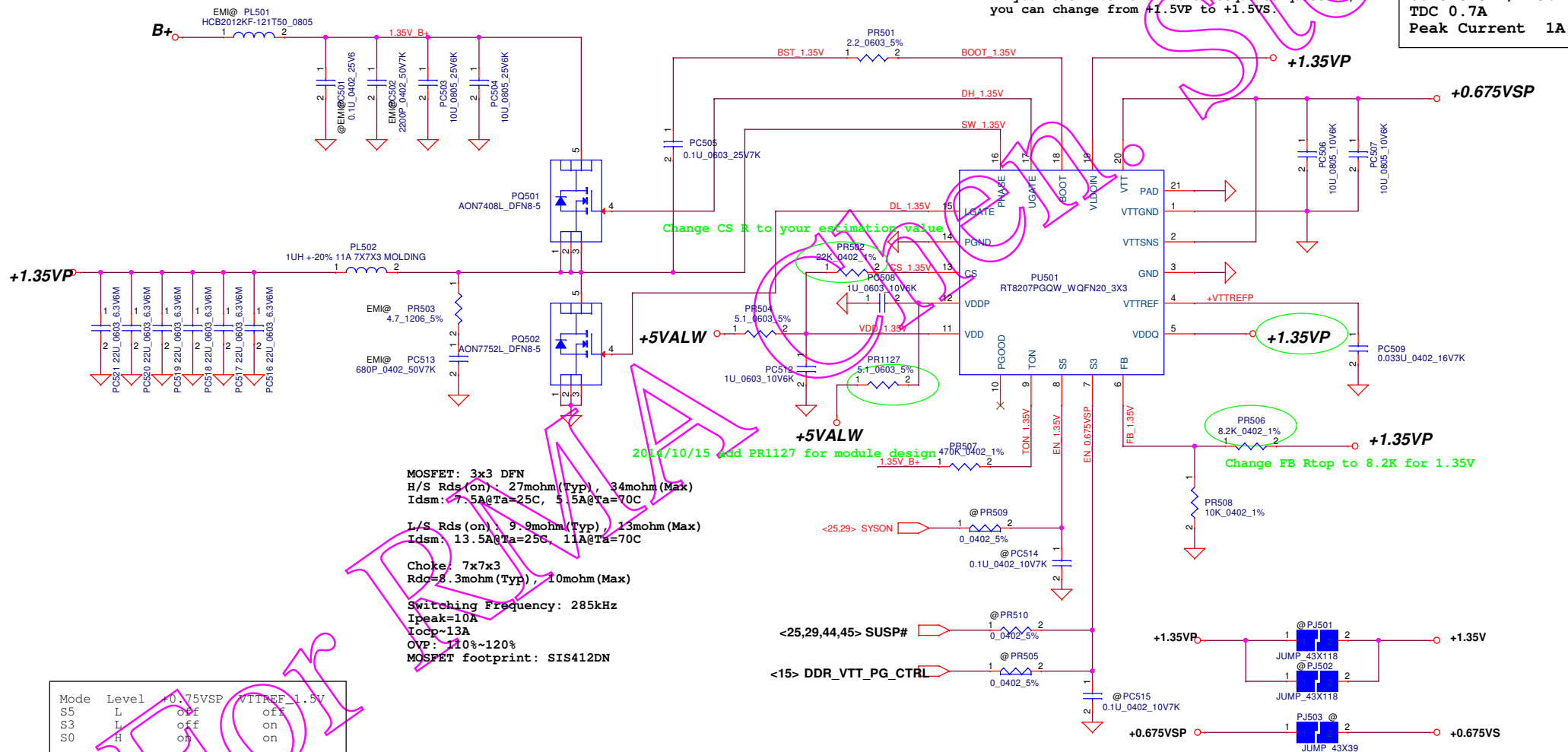


SY8208C_V2.mdd

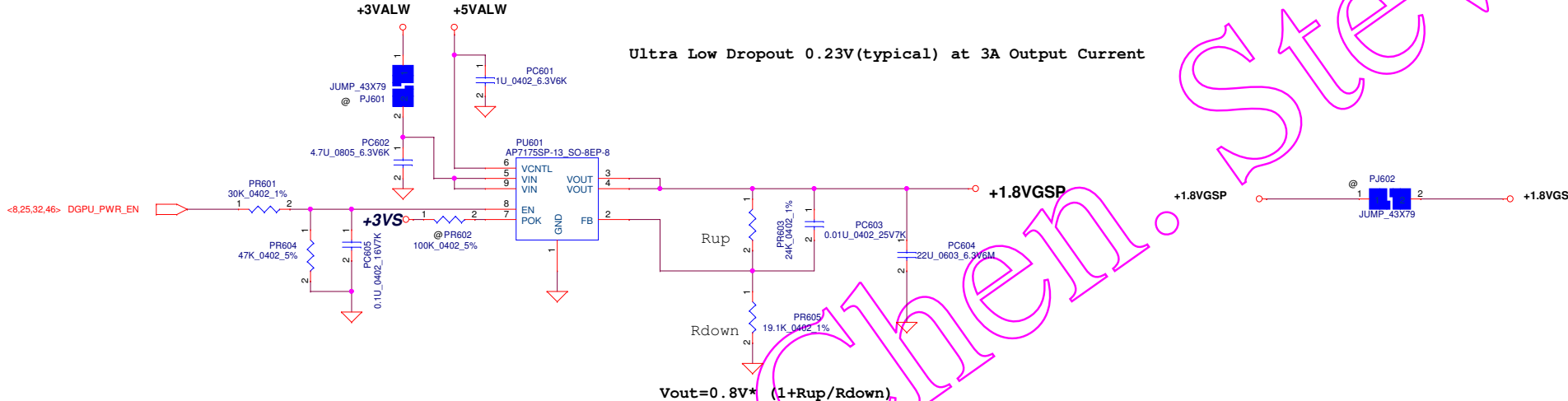
Compal Electronics, Inc.			
+3VALW/+5VALW			
Document Number	Z BDW		Rev 1.0
Edison	Edisonver 06 2015	Sheet 41 of 50	

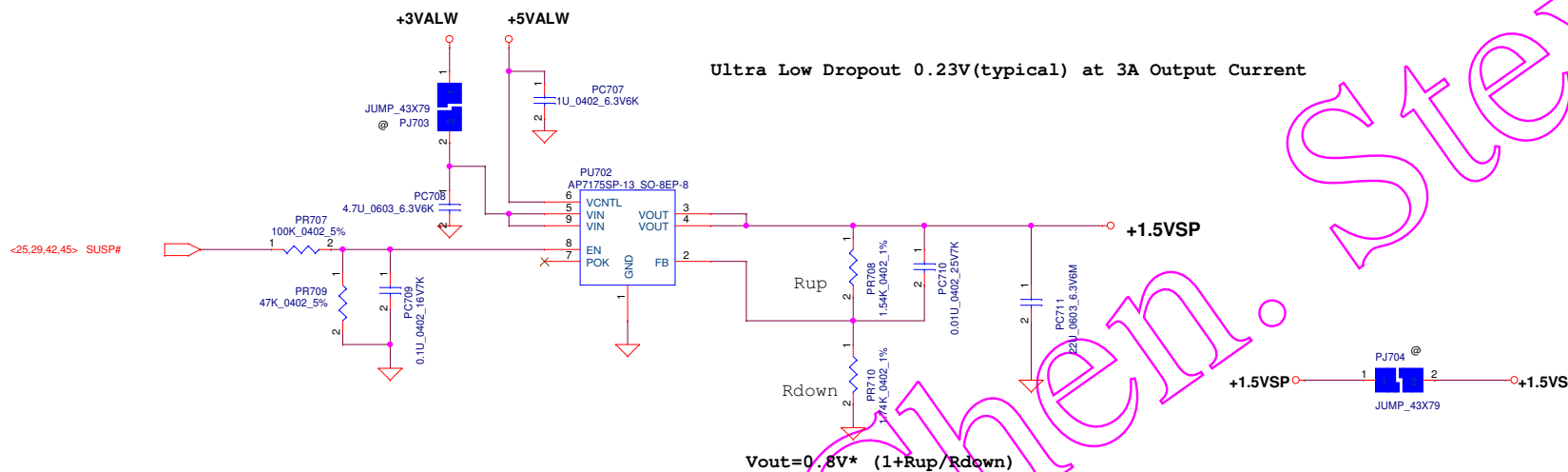
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer



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Custom	Z BDW				
Date:	Friday, February 06, 2015	Sheet	42	of	50

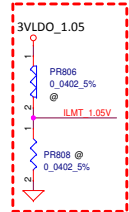




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```
Module model information
SY8208D_V1.mdd
```

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

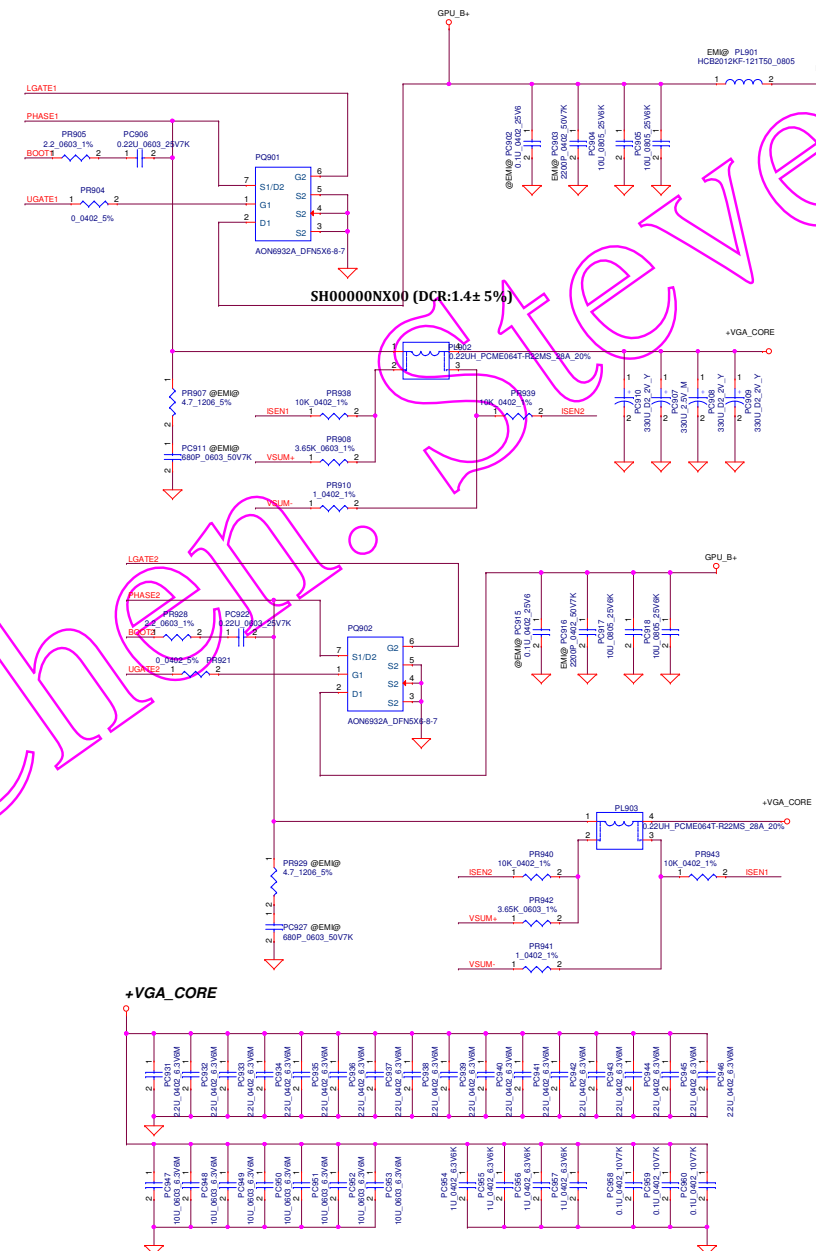
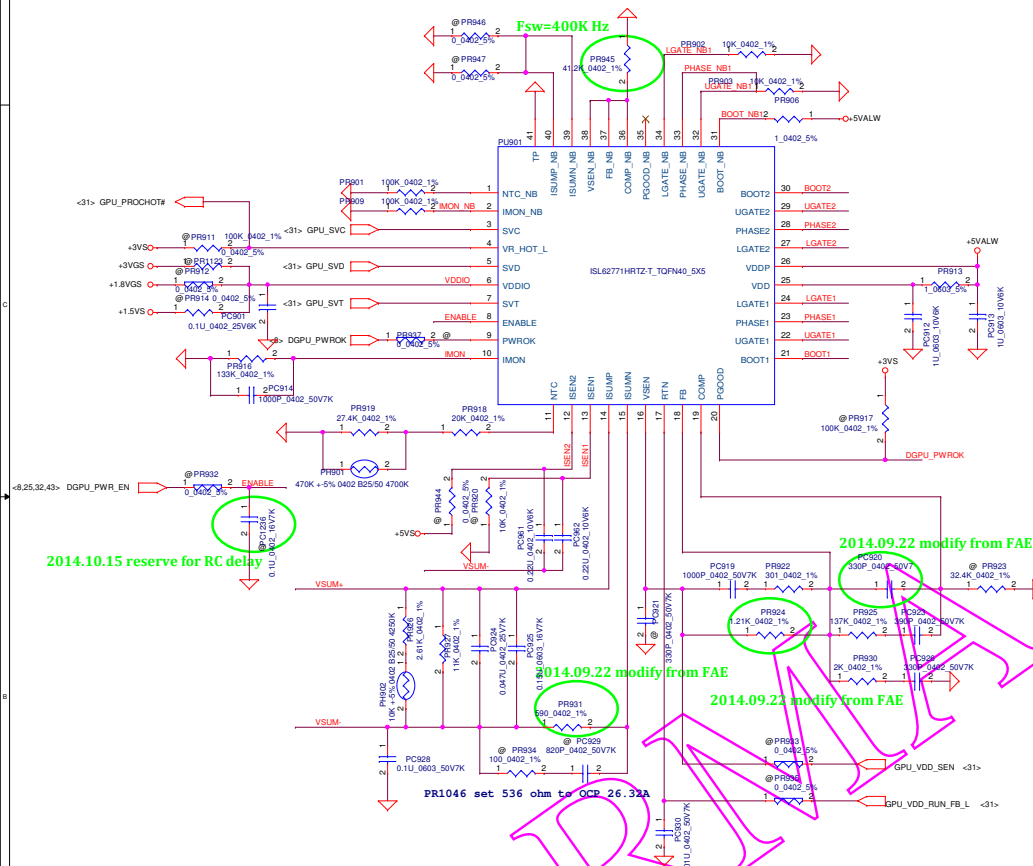
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

$$\begin{aligned} V_{FB} &= 0.6V \\ V_{out} &= 0.6V * (1 + R_{up}/R_{down}) \\ V_{out} &= 1.05V \end{aligned}$$

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Module model information
ISL62771_V1A.mdd for IC portion
ISL62771_V1B.mdd for SW portion

+VGA_CORE
AMD Meso XT
TDC 36A, EDC 54A
OCP min 67.8A



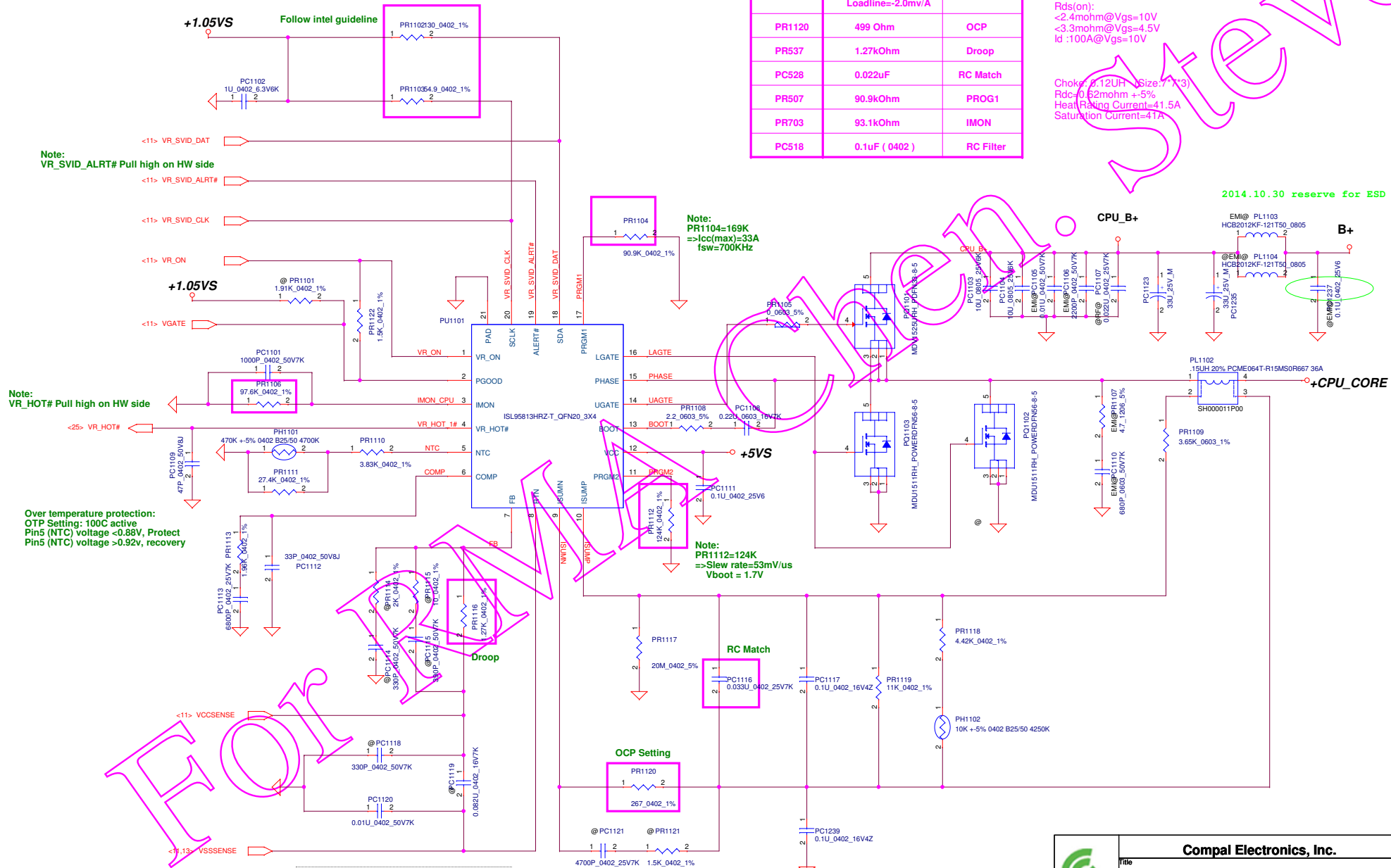
Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73		
Location	15W	Note
	TDC 14A	
	MAX 32A	
	OCp 39A	
	Loadline=-2.0mv/A	
PR1120	499 Ohm	OCp
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

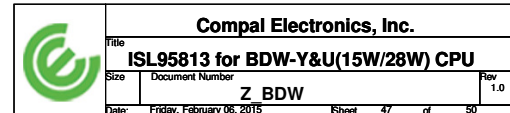
L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A

2014.10.30 reserve for ESD

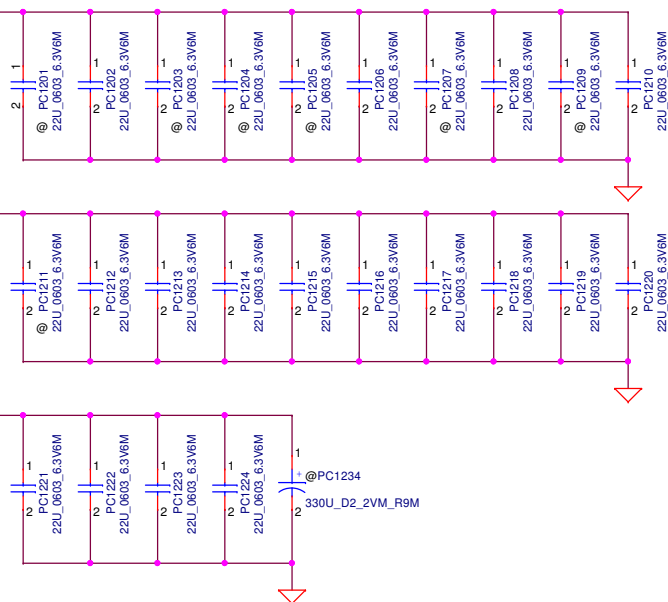


Local sense put on HW site



+CPU_CORE

24 X 22u/0603



For RMA

Chen. Steve

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				Date	Friday, February 06, 2015
				Sheet	48 of 50

Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	reserve VGA_CORE RC delay	P46	add PC1236	2014.10.15	SIV
2	reserve 0.1uF for ESD	P41/P47	add PC1237,PC1238	2014.10.30	SIV
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				BE BDW	
				Rev 1.0	
Date: Friday, February 06, 2015				Sheet 49 of 50	

Version change list (P.I.R. List)			Page 1 of 1 for HW		
Item	Reason for change	PG#	Modify List		Phase
1	Reserve clean CMOS circuit	P06	reserve R80,Q27	2014.10.28	SIV
2	HDMI Design	P18	add R1650,R1651,R1652,R1653,R1654,R1655,R1656,R1657,R1658,R1659,R1660,R1661	2014.10.28	SIV
3	USB2.0 design for EMI request	P24	add R1676 and R1677	2014.10.28	SIV
4	Change commom chock symbol for EMI request	P24	change L12~L18	2014.10.28	SIV
5	Add FAN_ID for EC request	P25	add R516 and R517	2014.10.29	SIV
6	Audio design for EMI request	P36	add CA28,CA29,CA30,CA31	2014.10.29	SIV
7	Audio design for EMI request	P36	change from RA19,RA20 to LA2,LA3	2014.10.29	SIV
8	Audio design for EMI request	P36	add LA1	2014.10.29	SIV
9	+1.35V design for EMI request	P15	add C320~C324	2014.10.29	SIV
10	modify +MEM_GFX power sequence	P32	change C901 from 0.01uF to 0.1uF	2014.10.30	SIV
11	LAN design change for wake on lan	P26	delete RL18, add J6,J7	2014.11.13	SIT
12	Change pcb foot print by DFX request	P20,P24	change J101,JODD1,JHDMI pcb footprint	2014.12.08	SIT
13	Change for VGA power sequence	P32	change CV35 value	2014.12.08	SIT
14	Change Audio PCBEEP SCH by verdor suggestion	P27	add RA35,RA37,CA90,CA91,RA39 / DELETE CA23,CA24,RA36,RA34,CA25	2014.12.15	SIT
15	Modify LED BOM setting	P27	modify LED1,LED2,LED3,LED4,LED5,LED6 BOM setting	2014.12.15	SIT
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